PHYSICAL STRUCTURAL AND BEHAVIORAL INTEGRATION OF GRAPHENE DEVICES

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PHYSICAL STRUCTURAL AND BEHAVIORAL INTEGRATION OF GRAPHENE DEVICES

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To my parents

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LIST OF SYMBOLS AND ABBREVIATIONS

g_m	transconductance
k	thermal conductivity
λ_F	Fermi wavelength
σ	electrical conductivity
ρ	resistivity
μ	mobility
E_F	Fermi energy
E_{gap}	bandgap
k_F	Fermi wavevector
V_{gs}	gate-to-source voltage
V_{dd}	power supply voltage
$V_{g,min}$	gate voltage at the minimum conductivity point
2DEG	2D electron gas
AFM	atomic force microscopy
ALU	arithmetic logic unit
BLG	bi-layer graphene
CMOS	complementary metal-oxide-semiconductor
CNT	carbon nanotube
CVD	chemical vapor deposition
EBL	electron-beam lithography
FET	field-effect transistor

FLG	few-layer graphene
GNR	graphene nanoribbon
HSQ	hydrogen silsesquioxane
I-V	current-voltage
ITRS	International Technology Roadmap for Semiconductors
LER	line edge roughness
QHE	quantum Hall effect
RF	radio-frequency
RIE	reactive ion etching
SEM	scanning electron microscope
SLG	single-layer graphene
VLSI	very large-scale-integration

SUMMARY

The strategic importance of microelectronics is reflected in its ubiquity in the global production network and in our daily lives. Above all, the microelectronics revolution has been enabled and driven by the scalability of the silicon transistor and the computational efficiency of its CMOS architecture. While the semiconductor industry has been incredibly adept at pushing the boundaries of scaling in the last few decades, many factors suggest that silicon technology is running into scientific and practical limitations to further scaling. Thus, the push for a beyond-silicon computing platform is imperative. Akin to the transition from bipolar to MOSFET technology or from NMOS to CMOS architecture, the industry is once again looking for the next disruptive technology to continue the exponential growth of computing power.

In 2004, two research groups, one from the University of Manchester and the other from Georgia Tech, reported on the electrical properties of ultrathin graphite. Their findings demonstrated the stability of graphene, an atomic layer of graphite, as well as its superb carrier mobility, spurring the semiconductor industry to invest in the material as a candidate for a beyond-silicon computing platform. Within this framework, this thesis explores the promise of graphene as a material and technological platform for electronic devices. The objectives of the thesis are (i) to elucidate opportunities and challenges in the design and fabrication of graphene field-effect devices, and (ii) to advance a new device platform based on graphene p-n junctions.

CHAPTER 1

INTRODUCTION

1.1 Justification of Research

Today, state-of-the-art microprocessors boast well over a billion transistors and are manufactured at the 22 nm technology node. For a little perspective, in 1971 the Intel 4004 microprocessor contained some 2300 transistors and was manufactured at the 10 μm technology node. Moore's Law, which pronounces the doubling of computing power every 24 months, has held remarkably well.

In the past, scaling entailed the reduction of physical dimensions of the transistor while leaving materials and the device structures basically intact. More recently, mere physical scaling has been supported by innovations in materials engineering and process integration. Metals have replaced poly-silicon as the gate material and hafnium-based dielectrics have replaced SiO_xN_y as the gate dielectric material. Germanium has been embedded into the silicon channel to improve carrier mobility (μ) of the channel. Non-planar transistors have recently been implemented at the 22 nm technology node. These innovations are projected to extend Moore's Law for several more years. Beyond that, the picture gets hazy. First, the dimensions of components of the transistor are approaching their physical limits [1]. As a result, devices suffer from poor reliability as minor process variations lead to major performance variations at the device and circuit level. Second, the manufacturing requirements of future technology nodes can only be supported by increasingly prohibitive costs. A fabrication facility at the 22 nm technology node costs

several billion USD [2]. Third, with the growth of mobile platforms and the cloud, the very meaning of computing is rapidly evolving [3]. Now, microprocessor design is not just about raw horsepower but rather about the tradeoff between performance and power efficiency. Taken together, these factors suggest that future advances in computing power will no longer be driven chiefly by the scaling of silicon but rather by the nexus of manufacturing and architectural innovations under a different computing paradigm. In silicon, these efforts range from device solutions such as transistors actuated by quantum mechanical tunneling currents to architectural solutions such as parallel computing to manufacturing solutions such as 3D-chip integration. Beyond silicon, opportunities for new computing paradigms are expanded. These include the integration of new materials and/or bottom-up manufacturing to circumvent (conventional) scaling issues to the use of new information carriers such as quantum mechanical spin. This thesis works toward a new computing paradigm from the latter perspective—the use of graphene as a material and technological platform for electronics.

Graphene is a single layer of carbon atoms arranged in a hexagonal lattice. From 0D buckyballs to 3D graphite, graphene is the building block of many carbon allotropes, Figure 1.1. Since the seminal studies on graphene in 2004, the scientific community has witnessed an outburst of interest in the material from theorists and experimentalists alike. In the first study [4], graphene was synthesized by mechanical cleaving of graphite (this type of graphene is known as “exfoliated graphene”). In the second study [5], graphene was synthesized by the sublimation of Si from SiC (this type of graphene is known as “epitaxial graphene on SiC”). Before these studies, physicists did not fathom that an atomically thin material could be isolated in the laboratory because of thermodynamic

instability [6]. Many research topics of quantum theory, previously limited to thought experiments or esoteric theory, became open to laboratory testing. More pertinently for electronics, graphene's high intrinsic mobility triggered the semiconductor industry to view graphene as a potential beyond-silicon semiconductor material.

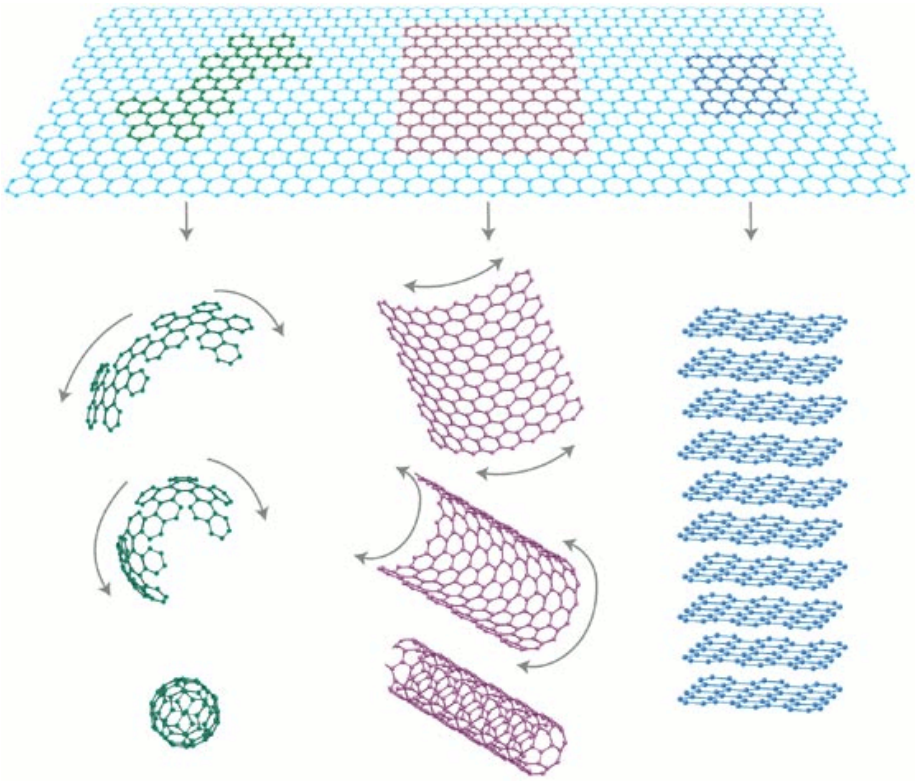

Figure 1.1: The allotropes of carbon. Graphene, a flat sheet of carbon atoms, forms the building block for 0D (buckeyballs), 1D (carbon nanotubes), and 3D (graphite) forms of carbon. Image from [7].

Among emerging research materials, what makes graphene uniquely competitive? After all, many other materials, including other two-dimensional electron gases (2DEGs) or carbon nanotubes (CNTs), have, in their time, also been hailed as a replacement for silicon. Compared with 2DEGs such as GaAs, phonon scattering is suppressed at elevated temperatures. Mobility in n-type GaAs-based semiconductors reaches 10^6 cm^2/V-s at T = 4 K but drops to a few thousand cm^2/V-s at room temperature [8]. By contrast, graphene

exhibits mobilities upward of 2×10^5 cm^2/V-s at room temperature [9], among the highest reported for any material. Further, the bandgap (E_{gap}) in 2DEGs, typically ~1 eV, creates a divergence of n- and p-type device characteristics [10]. Graphene's bandstructure, on the other hand, prescribes symmetric electron and hole behavior. For CNTs, the material remains vexed by low device density and poor controllability [11]. Graphene's planar geometry is more amenable for conventional top-down manufacturing.

The International Technology Roadmap for Semiconductors (ITRS) is a highly coordinated assessment of the semiconductor industry's future needs and prospects over the next 15 years. In its latest edition [12], the roadmap features graphene as both an emerging research device (for logic applications) and an emerging research material (for logic, interconnect, and metrology applications). *Stimulated by the historical imperative of Moore's Law and the fertile research in graphene, this thesis explores the promise of graphene as a material and technological platform for logic applications, engaging two themes.* In the first theme, challenges and opportunities in the design and fabrication of graphene field-effect devices are explored. The findings steer the direction and scope of the second theme—to consider a device platform based on graphene p-n junctions. This theme aims to advance a graphene device platform that goes beyond the field-effect device concept. In the rest of this chapter, perspective on silicon scaling and background on graphene are provided to contextualize the research.

1.2 Perspective on Silicon Scaling

A discussion of the historical scaling trends of the silicon field-effect transistor (FET) and its CMOS architecture serves to (i) give perspective on the semiconductor

industry and (ii) signal opportunities for a beyond-silicon computing platform. While Moore made the initial observation of doubling of chip functionality every year in the mid-1960s, it was Dennard [13] a decade later who transformed Moore's vision into an actionable roadmap by drafting scaling rules for silicon FETs, Table 1. In his paper, Dennard postulated that the scaling of device parameters such as the gate dielectric thickness, channel length, and power supply voltage (V_{dd}) would enable increasing chip functionality for a given area and power density. The technological and economic inertia of this roadmap is still with us today as the dimensions of current-generation transistors have scaled well below 100 nm.

Table 1: Dennard's scaling laws for silicon FETs

Device or Circuit Parameters	*Scaling Factor*
Device dimension t_{ox}, L, W	$1/\kappa$
Doping concentration N_a	κ
Voltage V	$1/\kappa$
Current I	$1/\kappa$
Capacitance $\varepsilon A/d$	$1/\kappa$
Delay time per circuit VC/I	$1/\kappa$
Power dissipation per circuit VI	$1/\kappa^2$
Power density VI/A	1

As discussed previously, the earlier generations of technology scaling generally followed the physical scaling described by Dennard. The problem is that, as transistors miniaturize into the deep sub-μm scale, certain assumptions about the performance and reliability no longer hold. To provide a couple examples of these scaling challenges, the design considerations for V_{dd} and channel thickness are discussed. The power supply

voltage has decreased with decreasing device dimensions (to maintain the strength of electric fields in the device), from 5 V at the 1 μm technology node in the 1980s to 1 V for the sub-100 nm technology nodes of today. Notably, dynamic power dissipation in silicon CMOS transistors is proportional to V_{dd}^2 while gate leakage power is proportional to V_{dd}. Thus although there are key benefits to more aggressive scaling, V_{dd} has not scaled as rapidly as device dimensions have. This is a consequence of the fundamental operating principles of the field-effect device. Specifically, the device's threshold voltage (i.e., the voltage needed to turn the device *on*) no longer scales; too low and the device is unable to turn *off*; too high and the transistor exhibits a poor *on* current. This scenario represents a fundamental design tradeoff between device speed and power dissipation. For the silicon channel, thickness has reduced with lateral scaling to maintain proper FET operation. In particular, the top-gate forms an inversion layer charge just below the surface of the silicon channel. As transistors shrink, channel thickness must also scale such that the channel is fully inverted under application of an external electric field. Otherwise, a significant leakage current flows through the "bulk" of the channel (the portion of the channel not inverted), thus hampering the ability to shut off the transistor. Critically, the scaling of channel thickness requires an increased doping concentration (not to mention the very precise positioning of these dopants) to minimize channel resistivity. In addition, the channel thickness for sub-100 nm technology nodes is below 10 nm. At such thin dimensions, carriers in the channel suffer from increased scattering off the silicon-to-silicon-dioxide interface and increased reliability issues from variability of the channel thickness and doping concentration. Herein, the complex interaction between device and processing requirements limits the ability to optimize for one without affecting the other.

Thus it is seen that physical scaling must now be accompanied by holistic systems scaling to sustain the pace of Moore's Law. For those interested in a detailed discussion on the historical development and future prospects for silicon/CMOS device design and process integration, there is extensive literature on the topic. See, for instance, documents from the ITRS or a series of papers from Khakifirooz and Antoniadis [14-16].

1.3 Graphene Fundamentals

Carbon has four electrons in its valence shell: one 2s and three 2p orbitals. In graphene, one 2s orbital and two 2p orbitals undergo sp^2 hybridization to form a trigonal planar geometry, Figure 1.2a. This geometry is responsible for the symmetric, hexagonal lattice of graphene (basal plane of graphene) in which strong sigma bonds form between carbon atoms. The remaining 2p orbital yields a distributed pi bond perpendicular to the graphene plane. The delocalized nature of the pi bond frees the corresponding electron from its host atom, and gives rise to graphene's high mobility and unique electronic properties. A mobility of 2×10^5 $cm^2/V\text{-}s$ in pristine graphene has been demonstrated at room temperature [17], signaling the prospect for ballistic, or scattering-free, transport on the μm-scale. The unit cell of graphene consists of two carbon atoms: one atom is part of sublattice A and the other is part of sublattice B, Figure 1.2a. The C-C bond length, a_0, is 1.42 Å[18]. $\mathbf{a_1}$ and $\mathbf{a_2}$ are the unit vectors of the lattice, where $\mathbf{a_1} = a_0/2\cdot\left(3\cdot\hat{\mathbf{x}}+\sqrt{3}\cdot\hat{\mathbf{y}}\right)$ and $\mathbf{a_2} = a_0/2\cdot\left(3\cdot\hat{\mathbf{x}}-\sqrt{3}\cdot\hat{\mathbf{y}}\right)$. Using this definition of a unit cell, a tight-binding calculation yields the following energy dispersion relation for low-energy carriers [18]:

$$E = \hbar\cdot v_F\cdot\sqrt{k_x^2+k_y^2} \tag{1.1}$$

where $v_F \sim 1\times10^6$ m/s. This energy dispersion is shown in Figure 1.2b. It is conical for low-energy carriers, and the intersection of the conical bands (conduction and valence bands) occurs at the six corners of the Brillouin zone, the so-called K-points or Dirac points. This unique energy dispersion has several important outcomes. First, graphene does not have a bandgap; it behaves as a semi-metal (not quite a semiconductor but not quite a metal either). Second, these conical bands direct carriers in graphene to behave like relativistic particles (i.e., Dirac particles) that travel at $1/300^{th}$ the speed of light. This conical energy dispersion holds until the energy of the carriers deviates by $\geq$ 200 meV from the Dirac point [19]. Third, in intrinsic (undoped) graphene, the Fermi energy (E_F) resides exactly at the Dirac point, suggesting that intrinsic graphene is insulating since there are no available states at the Fermi energy. In actuality, any finite temperature elevates electrons (holes) to the conduction (valence) band. In addition to thermal energy, perturbations to the graphene lattice, either imperfections in the lattice itself or through the influence of neighboring materials, dope graphene and shift E_F away from the Dirac point. It is this rich plasticity and high carrier mobility that make graphene such an intriguing material for electronics.

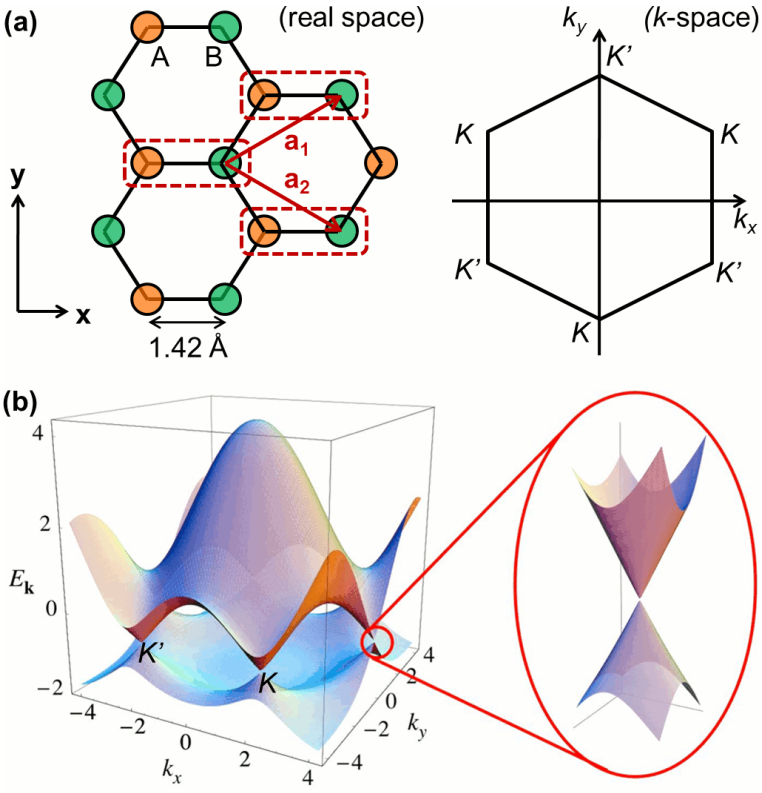

Figure 1.2: Graphene's crystal lattice and bandstructure. In (a), the real and momentum space representations of the crystal structure are depicted. The equivalency of the A and B sublattices results from the two-atom unit cell in graphene. The corresponding energy dispersion (which is conical for low-energy carriers), from tight-binding calculations, is shown in (b) [20]. This energy dispersion has important consequences for carriers in graphene, including semi-metallic transport behavior, high carrier mobility, and photon-like properties.

Expression of the quantum Hall effect (QHE)—quantization of energy levels under an external magnetic field—in graphene [21, 22] presented experimental validation that its charge carriers behave as Dirac particles. In contrast to conventional 2D systems, in graphene the quantization condition occurs at half-integer rather than integer values. In addition to the half-integer QHE, graphene exhibits a fractional QHE [23, 24] as a result of the collective behavior of its charge carriers. The results of these experiments remain, for now, under the domain of physics rather than engineering owing to the need for a

highly ideal experimental apparatus. The observation of a room-temperature mobility of 2×10^5 $cm^2/V\text{-}s$ [17] and the fractional QHE [23, 24] requires the fabrication of ultra-pristine graphene through suspension of the graphene layer. This is followed by cleaning methods to reduce external scattering sources and the need for a delicate test setup. In more practical devices, extrinsic disorder is certain to govern transport properties. In any case, these highly-controlled experiments are valuable because they provide insight into the performance limits of intrinsic graphene.

A relaxation of the ideal properties of graphene is necessary on consideration of two points. First, devices are of technological interest for very-large-scale-integration (VLSI) chips only if they can be scaled down to the sub-μm regime. Second, graphene synthesis and device processing are imperfect and result in disordered or polycrystalline graphene. As a simple example, a scalable graphene device can be constructed by way of a ribbon structure. A graphene ribbon is defined by the chiral vector $\mathbf{C} = (m,n) = m\cdot\mathbf{a_1} + n\cdot\mathbf{a_2}$, where $\mathbf{a_1}$ and $\mathbf{a_2}$ are the unit vectors of graphene and m and n are integers (Figure 1.3). The electronic properties of a graphene ribbon depend on its size and edge structure [25]; the ribbon edges take on zigzag form, armchair form, or a mixture of the two. For armchair edges, a graphene ribbon is either metallic or semiconducting depending on the number of carbon atoms across its width (N). It is metallic for $N = 3\cdot M - 1$ and M is an integer, and semiconducting otherwise. For zigzag edges, a graphene ribbon is metallic for all widths. In general, line edge roughness (LER) washes out the ability to fabricate purely zigzag or purely armchair ribbons as actual edge composition becomes a mixture of zigzag and armchair patterns.

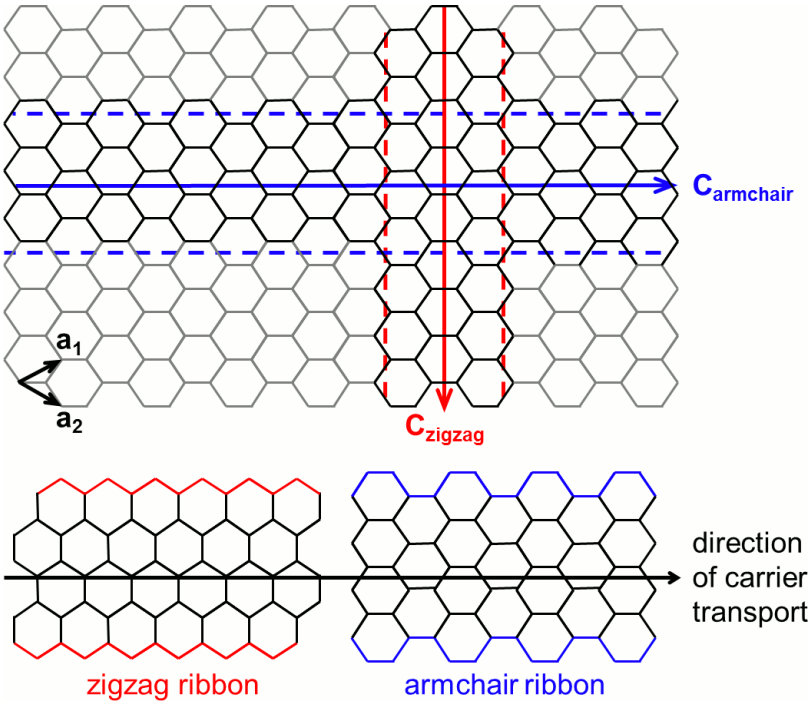

Figure 1.3: Edge configuration in graphene ribbons. 2D, large-area graphene can be cut into 1D, graphene nanoribbons defined by its chiral vector, $\mathbf{C} = (m,n) = m \cdot \mathbf{a_1} + n \cdot \mathbf{a_2}$. While transport properties depend on edge configuration, manufacturing limitations result in ribbons with a mixture of zigzag and armchair edges rather than purely zigzag or purely armchair edges.

This section concludes with a review of some of graphene's superlative properties outside of the electrical domain. While the work herein focuses on logic applications for graphene, a broader understanding of the material is needed for process integration. For instance, how do its thermal and mechanical properties support its electronic properties? With a thermal conductivity greater than that of diamond [26], large-area graphene is being explored as a heat spreading material. Despite its atomic flatness, graphene has a Young's modulus of 1000 GPa [27], five times that of steel, making it attractive as a lightweight strengthener for composites. Graphene has a high optical transparency—a single layer absorbs just 2.3% of white light [28]. This absorbance level can be viewed either as small or significant, depending on the thickness of graphene used. Single-layer

graphene (SLG) can be used for transparent films and few-layer graphene (FLG) can be used for opaque films. Lastly, given its atomically thin nature (a single layer of graphene is just 3.34 Å thin), graphene opens up many possibilities for sensing.

1.4 Scattering Mechanisms in Graphene

The intense research activity on graphene devices has brought forth a workable understanding of electronic transport in graphene. While intrinsic graphene exhibits a room-temperature mobility of ~10^5 cm^2/V-s, the majority of devices tested in typical laboratory environments demonstrated mobilities in the range of 10^3–10^4 cm^2/V-s. The discrepancy was due to various scattering sources—impurities found in the supporting substrate or other surrounding media, remote phonons from the surrounding dielectric, adsorbates from the atmosphere, or disorder in the graphene itself. In this section, the impact of various scattering mechanisms on carrier transport in graphene is discussed.

The majority of the early device experiments were carried out on the exfoliated graphene platform (graphene flakes on SiO_2 that is thermally grown on a doped silicon substrate). This SiO_2 film, which doubles as a dielectric layer for electrical gating, introduces scattering from impurities and remote phonons, and imparts microscopic ripples onto the graphene film. First, and most significantly, impurities at the graphene-substrate interface increase the scattering cross-section of carriers in graphene. For most devices, this scattering source is the most dominant and limits mobility to 10^3–10^4 cm^2/V-s [29]. Second, scattering from remote phonons in the SiO_2 limits graphene's mobility to 4×10^4 cm^2/V-s at room temperature [17]. This scattering mechanism, while not as significant as impurity scattering, represents a theoretical limit on the performance of

graphene devices on a SiO_2 substrate. Finally, graphene conforms to undulations of the substrate, breaking the symmetry of the lattice and contributing to additional scattering [30]. A study of graphene on hexagonal boron nitride (whose surface is smoother than that of SiO_2) [31] suggests that ripple scattering plays a minor role in comparison with impurity or remote phonon scattering. As graphene devices progressed from simple two-terminal structures toward three-terminal, gated structures, the added device complexity introduced more scattering sources. Top-gate dielectrics compounded the influence of back-gate dielectrics. Contact electrodes dope graphene by injecting electrons or holes into the device, depending on the metal's work function [32]. Charge transfer occurs through atmospheric contaminates that adsorb onto graphene [33]. The impact of this charge transfer, which results in hole-doping of graphene, has been observed repeatedly in experiments (see Chapter 5).

The scattering sources described so far have focused on "extrinsic" sources, i.e. scattering sources that arise from neighboring materials (such as a contact electrode or dielectric film) or adsorbates (such as adatoms). Next, "intrinsic" scattering sources that arise from structural imperfections in the graphene lattice are discussed. These include non-hexagonal carbon rings (such as pentagon-heptagon pairs), vacancies, dislocations, substitution atoms [34]. These defects result in either a change in the local electronic structure or an injection of charges to the lattice. Not surprisingly, the density of intrinsic defects depends to a large extent on the method for graphene synthesis. In exfoliated graphene, intrinsic defect density is found to be less than 1×10^{10} cm^{-2} [9], confirming high crystalline order. In epitaxial growth—via chemical vapor deposition (CVD) on metal substrates [35] or the sublimation of Si on SiC [5]—graphene forms out of multiple

nucleation sites, leading to an increased defect density [36, 37]. Clearly, it is vital to merge the high quality of exfoliated graphene with the large-scale manufacturability of CVD-grown or epitaxial graphene. In addition to their influence on transport, structural defects in graphene are noted for the following reasons. First, the type and density of structural defects determine a material's mechanical strength. Second, structural defects break the symmetry of graphene's lattice. This disrupts graphene's tendency to remain inert and thus provides opportunities for tailoring of its transport properties. For example, periodic line dislocations, if intentionally patterned, can be used to convert the areas from semi-metallic graphene to insulating graphene (by altering sp^2-bonded carbon to sp^3-bonded carbon). The role of various scattering sources (the impact of edge scattering is neglected) across graphene platforms is shown qualitatively using material resistivity (ρ) in Figure 1.4.

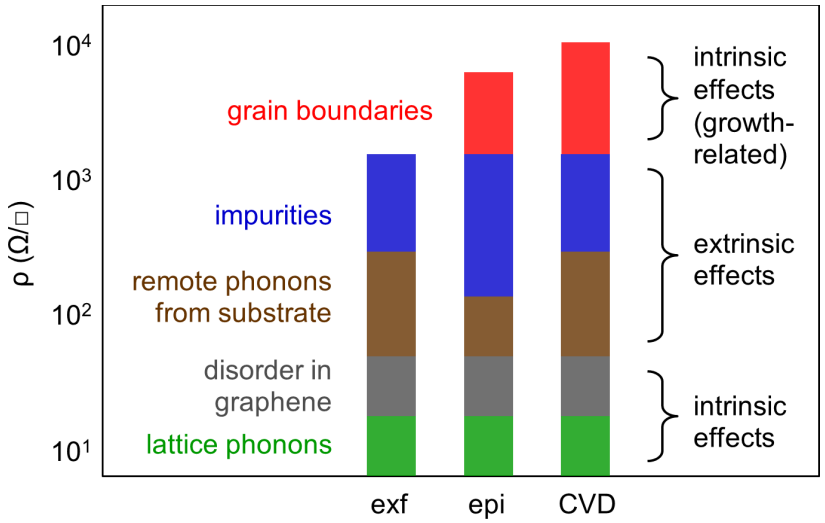

Figure 1.4: Role of various scattering sources in graphene. There are several methods to synthesize graphene; "exf" designates exfoliated graphene on SiO_2, "epi" designates epitaxial graphene on SiC, and "CVD" designates CVD-grown graphene transferred onto SiO_2. Resistivity is shown qualitatively for a carrier density of 1×10^{12} cm^{-2} at T = 300 K. While exfoliated graphene offers higher-quality starting material, the epitaxial or CVD-grown graphene platforms are more amenable to large-scale manuf acturing.

1.5 Graphene Field-Effect Transistors

The first electrical transport measurements on graphene [4, 5] exhibited the behavior of a zero-bandgap semi-metal: devices exhibited a high conductivity (σ) but only a modest carrier modulation (< 10). Without a bandgap, it was not possible to switch off current to a level that is sufficient for digital switching. As these early experiments were all carried out on 2D, large-area graphene (dimensions > 1 μm), it was of interest to repeat these measurements for 1D, graphene nanoribbons (GNRs), where confinement of carriers to a single dimension is expected to open a bandgap [38]:

$$E_{gap} \approx a/W \tag{1.2}$$

where $a \sim 1$, E_{gap} is expressed in eV, and GNR width W is expressed in nm. The first set of experiments revealed a E_{gap} larger than predicted—Han *et al.* [39] attained $a \sim 5$. This discrepancy is now attributed to the observation of a transport gap [40], not a bandgap. A transport gap, simply put, is a measure of the size of the low-conductance state of a device. In ordered systems, the transport gap equals the bandgap; in disordered systems, the transport gap is larger than the bandgap. For GNRs, impurities in the substrate break up graphene into distinct islands of charge puddles [41, 42]. Carriers no longer travel through an ordered crystal lattice with little scattering but rather through a patchwork of graphene grains. Consequently, transport measurements in these GNRs probe the inter-grain properties in addition to the intrinsic properties of graphene (within a grain). In an ordered system, GNRs with a small degree of LER would in fact exhibit a smaller than predicted E_{gap}. This effect appears since edge roughness (from manufacturing limitations) results in the mixing of edge states that, in turn, leads to the elevation of semiconducting states and the suppression of metallic states [43]. It is thus seen that disorder (arising

from impurities or edge roughness) presents challenges to the suitability of GNRs for logic applications. In addition, ultra-narrow GNRs ($W < 10$ nm) yield a sizeable E_{gap} but also a reduced performance; this tradeoff reflects the inverse correlation of bandgap and mobility for semiconductors [44]. At these dimensions, intrinsic phonon scattering plays a heightened role relative to external scattering sources. These concepts are explored in greater detail in the size effect study of Chapter 4.

The desire to study more practical transistors required a shift from the facile back-gate setup of the early experiments toward a top-gate setup. This succeeding iteration of graphene transistors involved a top-gate setup with SiO_2 as the gate dielectric. Further development featured Al_2O_3 and HfO_2 as high-κ gate dielectrics. In a work by Liao *et al.* [45], Al_2O_3 nanoribbons functioned as a top-gate dielectric and yielded a mobility of 2.4×10^4 $cm^2/V\text{-}s$. This experiment and others with HfO_2 as the gate dielectric [46, 47] demonstrated the compatibility of graphene with high-κ gate dielectrics.

1.6 Alternative Device Platforms

The application of graphene nanoribbons as the channel material for FETs has definite advantages: the ability to modify E_{gap} and the adoption of the top-down, silicon manufacturing paradigm toward graphene. In this section, two other device platforms are discussed: bandgap tuning in bi-layer graphene (BLG) and the Klein tunneling effect in single- and bi-layer graphene.

The unique energy dispersion of bi-layer graphene opens up various avenues to design logic switching mechanisms. In BLG, the two graphene layers exhibit Bernal stacking (the same stacking order as for graphite): the lattice of the top layer is shifted

with respect to that of the bottom layer such that half of the atoms in the top layer are located above the center of the hexagonal rings in the bottom layer. In this configuration, inversion symmetry holds between the two layers and BLG behaves, like SLG, as a zero-gap semi-metal. A perturbation of the stacking order (e.g., by inducing an electric field through gating) breaks this symmetry since carbon atoms in the top layer experience a different potential than carbon atoms in the bottom layer. The breaking of the inversion symmetry induces a bandgap in BLG that can be tuned by varying the strength of the perturbation (by varying the applied gate voltage). In [48], a top- and bottom-gate were used to attain E_{gap} of 250 meV and $I_{on}/I_{off} > 10^3$, illustrating a pathway for the use of graphene FETs. A challenge of this method is the added complexity of the double-gate structure that is required to independently tune E_{gap} and carrier density. An alternative implementation could be through the combined use of a single-gate and a dopant layer adjacent to graphene (that plays the role of a second gate). In this manner, the key parameter of the dopant layer—its doping density—is chosen to optimize E_{gap} and the single-gate is used to control the carrier density and operate the device.

In a way, the graphene FET can be viewed as a constraint for graphene electronics since it is based on the principles of the silicon FET and does not necessarily make use of the properties of graphene. Put differently, the pursuit of graphene electronics demands not just an understanding of material properties but the integration of material, device, and architectural solutions into a new computing platform. It is thus essential to consider the physics of graphene to imagine a more suitable device concept. A unique feature of graphene is the angle-dependent tunneling behavior of its charge carriers; this is the so-called Klein paradox [49]. The Klein paradox describes quantum mechanical tunneling

for relativistic particles. In the context of graphene [50, 51], this tunneling effect predicts that carriers striking an energy barrier (at normal incidence) attain complete transmission through the barrier in single-layer graphene but witness complete reflection in bi-layer graphene. In SLG, the wavefunction of a propagating electron outside the energy barrier matches that of a propagating hole inside the barrier, preserving transport. In BLG, the wavefunction of a propagating electron outside the barrier matches that of an evanascent wave inside the barrier, disrupting transport. This peculiarity is a result of charge-conjugation symmetry, which arises from the material's crystal symmetry. Although the transmission probability is influenced by the height and width of the barrier, it depends more appreciably on the carrier's incident angle. Carriers that strike the barrier away from normal incidence witness the collapse of the Klein effect: perfect transmission (reflection) no longer holds for SLG (BLG). This unique tunneling behavior for carriers in graphene can be used to construct a switching device that circumvents the issue of a lack of bandgap, merging the material's high mobility with an excellent on/off current ratio (see Chapter 6).

1.7 Organization of Thesis

Continued growth of the semiconductor industry depends on either the sustained progress of silicon or the development of a beyond-silicon computing platform. With traditional device scaling in silicon becoming increasingly more difficult, there has been a refocusing on manufacturing innovations (including new materials) and architectural innovations. The work herein focuses not on the scalability of silicon as the channel material but rather on the possibility of using a different channel material. *Within this*

framework, this thesis explores the promise of graphene as a material and technological platform for electronic devices, engaging two themes. In the first theme, comprised of four tasks, opportunities and challenges in the design and fabrication of graphene FETs are elucidated. First, a work flow for the design, fabrication, and characterization of graphene devices is developed (Chapter 2). Second, the current-carrying capacity and thermal conductivity of GNRs are investigated (Chapter 3). Third, the electrical impact of the size effect—the modification of properties at reduced dimensions—in nanoscale graphene devices is studied to understand their scaling limits (Chapter 4). Fourth, variation in graphene devices is investigated (Chapter 5) by measuring the response of graphene to (i) atmospheric adsorbates (composed of molecular oxygen and water) in exfoliated graphene on SiO_2 and (ii) substrate-induced disorder in epitaxial graphene on SiC. Taken together, the findings of these four tasks provide insight into physical and structural properties of graphene field-effect devices. Further, they help recognize the direction and scope of the second theme—to advance a device concept more suited to the unique physics of graphene. The candidate device platform operates on the principle of Klein tunneling, a tunneling effect predicted for carriers in graphene (Chapter 6). In Chapter 7, a research summary, future work, and prospects for graphene are discussed.

CHAPTER 2

TECHNOLOGY DEVELOPMENT OF GRAPHENE DEVICES

2.1 Introduction

The suitability of graphene as a material and technological platform for logic devices hinges upon delivering superb device-, circuit-, and system-level performance at reasonable cost. Additionally, the exploration of a new material provides the opportunity to rethink device and architectural solutions. Such a device platform based on graphene would need to be supported by three pillars (Figure 2.1): semiconductor device design to address the unique physics of graphene, synthesis and nanoscale fabrication techniques to develop a process flow for graphene devices, and electrical and structural testing methods to analyze graphene's device properties.

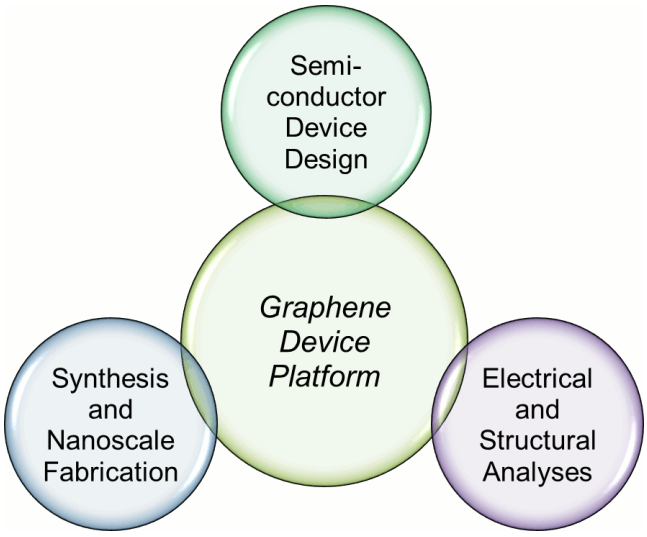

Figure 2.1: Functional themes of the work of this thesis. A graphene device platform is developed and supported by three pillars: semiconductor device design, synthesis and nanoscale fabrication, and electrical and structural analyses.

With graphene, new process and characterization methods are needed to control and investigate the exotic material. From a processing perspective, the atomically thin nature of the material presents at once a great opportunity and a great challenge. The first task of this thesis is to develop a work flow—encompassing design, fabrication, and testing methods—for graphene devices, thus enabling the study of various device structures presented later in the thesis. In the bulk of this work, exfoliated graphene is used since it has a lower defect density compared with epitaxial graphene. On the other hand, it is also important to understand key transport differences between exfoliated and epitaxial graphene since the latter platform offers a more feasible route toward large-scale manufacturing. There are two primary methods for epitaxial graphene growth: an additive process via CVD on metal and a subtractive process via sublimation of Si from SiC. Among the two epitaxial platforms, this work uses epitaxial graphene on SiC (hereafter referred to simply as epitaxial graphene) since it provides ready access to a high-bandgap semi-insulating substrate for device fabrication. For CVD-grown graphene, the material must be transferred from a metal substrate (needed during the growth process) onto an insulating or semiconducting substrate before device fabrication. This transfer process, however, introduces additional impurities into the graphene film.

Graphene devices are patterned using an assortment of configurations—from a Hall bar structure on large-area graphene to a wire structure using a graphene ribbon to a three-terminal (gated) device—to understand different aspects of graphene's electrical behavior. For instance, Hall bar testing on large-area graphene reveals intrinsic material properties while gate testing uncovers field-effect device characteristics. The fabrication methods used in this thesis are initially developed for an exfoliated graphene FET. The

fabrication process for both epitaxial graphene devices (Section 2.4) and graphene p-n junction devices (Chapter 6) builds upon the exfoliated graphene FET process flow.

2.2 Fabrication Process Flow for Exfoliated Graphene Devices

In the exfoliated graphene platform, the synthesis of graphene uses the "scotch tape" method—that is, the mechanical cleaving of graphene flakes from graphite. As the name of the method suggests, tape is used to thin down bulk graphite (Kish A, purchased from Toshiba Ceramics) to ultrathin graphite flakes, which includes single-, bi-, and few-layer graphene. Then, the graphene flakes (named so because of their size, typically 10−100 μm^2) are transferred from the tape onto thermally-grown SiO_2 atop a p++ doped silicon substrate, Figure 2.2a. This transfer is promoted by Van der Waals forces between the flakes and the substrate. The supporting oxide also functions as a gate dielectric (with silicon as the back-gate) during electrical testing. The specified oxide thickness (either 90 or 300 nm) is chosen to provide sufficient optical contrast between the graphene flakes and the SiO_2 substrate (a single layer of graphene absorbs 2.3% of white light [28]). The position of the deposited flakes is measured relative to a pre-patterned grid of alignment markers (patterned via photolithography and a metal liftoff step); these coordinates are used for alignment in subsequent lithography steps. Raman analysis verifies the thickness and quality of the film by inspection of the D-, G-, and 2D-bands at approx. 1350, 1580, and 2700 cm^{-1}, respectively (Figure 2.2b). Thicker graphene has a wider and upshifted 2D-band, while the ratio of the peak intensity of the 2D-band to that of the G-band decreases. Raman analysis is sensitive to the thickness of graphene up to five layers [52]. Atomic Force Microscopy (AFM) further supports the results of Raman analysis.

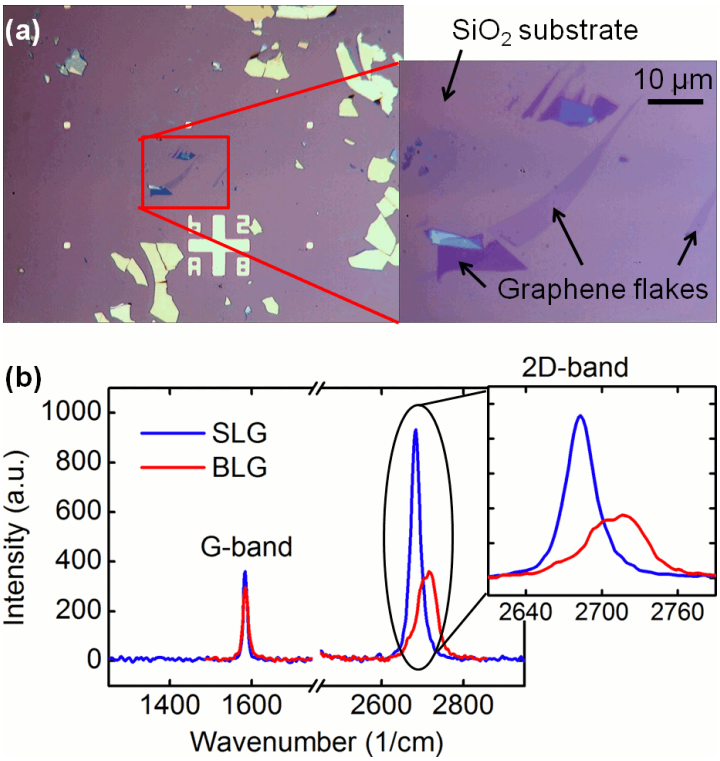

Figure 2.2: Synthesis and characterization of exfoliated graphene. In (a), optical images reveal graphene flakes (from mechanical cleaving of bulk graphite) onto a substrate of a 90 or 300 nm thick film of SiO_2 atop degenerately-doped silicon. In (b), Raman analysis reveals the difference in single- and bi-layer graphene. For SLG, the width of the 2D-band is sharper while the ratio of the peak intensity of the 2D-band to that of the G-band is much greater. In either case, the lack of a D-band (at 1350 cm^{-1}) indicates high-quality graphene.

After identification of high-quality graphene flakes, electron-beam lithography (EBL) (using a JEOL JBX-9300FS system) with positive-tone resist, ZEP520 (Zeon Chemicals) is used to pattern contact electrodes. An e-beam evaporation and metal liftoff process is then used to deposit the contact electrodes onto the graphene flakes. The metal stack is comprised of Ti as the adhesion layer and Au as the bulk layer for improved conductivity. After metal deposition, the resist and the overlaying metal is rinsed away using microposit remover 1165 (Shipley Company). A second EBL step with negative-tone resist, hydrogen silsesquioxane (HSQ, purchased from Dow Corning), is used to

define a resist mask for the desired graphene structures. An argon plasma etch is used to transfer the resist pattern into graphene. Afterward, the HSQ structures atop graphene can be removed using hydrofluoric acid (HF) though this is not typically done since HF would also etch the oxide substrate. This exfoliated graphene fabrication process flow for a three-terminal, back-gated device is shown in Figure 2.3. In addition, a top-gate process is developed to allow local electrostatic control of the graphene device, in contrast to the global control by the back-gate. For a more detailed description of the workflow and characterization methods for graphene devices, refer to Appendix A.

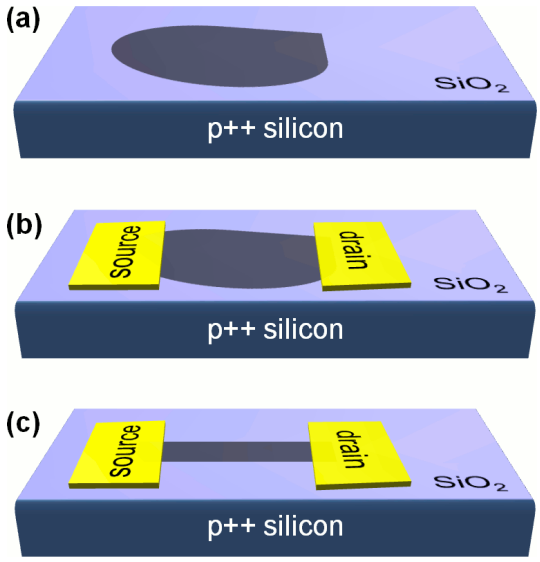

Figure 2.3: Exfoliated graphene fabrication process flow for a three-terminal, back-gated device. In (a), high-quality graphene flakes are deposited onto a 90 or 300 nm thick film of SiO_2 and then identified by optical microscopy. In (b), e-beam lithography, e-beam evaporation, and metal liftoff are used to pattern contact electrodes (Ti as the adhesion layer and Au as the bulk layer). Finally, in (c), a second e-beam lithography step and an argon plasma forms the desired graphene structures.

2.3 Process Integration for Exfoliated Graphene Devices

The previous section outlined the fabrication process for graphene devices on the exfoliated graphene platform. This section discusses the process integration required to

achieve high-quality graphene devices, which includes various cleaning steps, tuning of the plasma etch, and layout design of contact electrodes to mitigate their doping effect on graphene.

In exfoliated graphene, substrate cleaning (before exfoliation takes place) helps minimize substrate doping. This involves a descum process using a low-power O_2 plasma to remove organic residue from the surface. This is a critical step because such residue gives rise to impurities trapped at the graphene-substrate interface, a dominant scattering source in graphene [29]. The presence of these impurities is permitted by the surface chemistry of the substrate. For SiO_2, hydroxyl groups (–OH) react with dangling Si bonds on the surface that leads to a layer of silanol (SiOH) groups [53]. The silanol groups, in turn, react with dipolar molecules such as water that contribute to scattering in graphene. Using AFM, the surface roughness of the substrate was compared after two different clean methods—an acentone-methanol-isopropanol (AMI) rinse and a descum process, Figure 2.4. This confirmed that the SiO_2 substrate remained smooth after the descum process. (A third clean method was attempted using dilute HF; this caused the surface roughness to increase significantly.) Afterward, devices are baked inside a vacuum oven (~10 Torr) at 300–400 ˚C. This baking step dehydrates the surface of the SiO_2 and helps reduce doping from adsorbates. As the SiO_2 substrate is prepared for exfoliation, scotch tape with peeled graphene flakes are prepared in advance. Then, once the substrates are retrieved from the oven, the graphene flakes can be deposited onto the devices while they are still warm (above 100 ˚C), reducing the possibility of contaminants getting trapped at the graphene-SiO_2 interface.

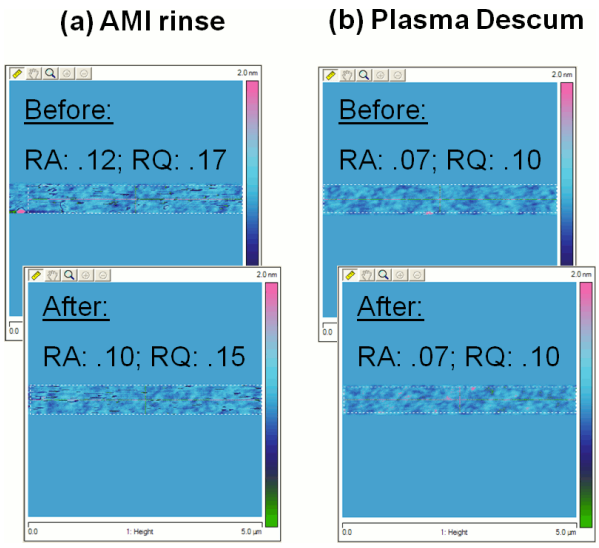

Figure 2.4: AFM scans of the SiO_2 substrate after substrate cleans. In (a), an AMI rinse is used while, in (b), a descum process is used. The surface roughness after each clean method is comparable.

After preparation of high-quality graphene onto a clean SiO_2 substrate, an EBL step and a metal liftoff process are used to pattern contact electrodes onto the flakes. The metal stack is chosen with Ti as the adhesion layer and Au as the bulk layer for improved conductivity. Electrical measurements across large-area graphene flakes revealed ohmic contacts. Initially, both Pd and Ti were considered as the adhesion metal. However, the choice of electrode material affects the doping of graphene adjacent to the electrodes because of a mismatch between the metal and graphene work functions. Pd (with a work function of 5.12 eV [54]) hole-dopes graphene (work function of ~4.6 eV [55]) while Ti (work function of 4.33 eV [54]) electron-dopes graphene. Doping of graphene from the contacts is less severe with Ti as the adhesion layer since Ti has a smaller work function difference with graphene than Pd does. For this reason, Ti is chosen as the adhesion layer metal. Based on test devices of different lengths in this work, it is seen that the doping from the metal is severe for the graphene regions less than 100 nm from the electrode

edges. Thus, where possible, graphene devices are positioned at least 100 nm away from contact electrodes to minimize any charge transfer from metal to graphene.

In the second patterning step, e-beam lithography and a subsequent plasma etch are used to pattern the desired graphene structures. With the JEOL JBX-9300FS EBL system, an e-beam energy and current of 100 keV and 2 nA, respectively, are employed. An important consideration for EBL patterning is the proximity effect, whereby electron scattering in the resist and substrate leads to exposure in regions of the resist outside the intended patterning area [56]. Since this effect becomes more pronounced for smaller patterns, it is especially relevant for the graphene devices of this work (with dimensions in the sub-μm scale). Experiments were thus carried out to determine suitable e-beam doses for patterning graphene nanoribbons with a range of widths.

Optimization of the plasma etch step calls for the minimum effort to ensure full etching of the graphene flakes. With additional etching past this threshold point, HSQ (the resist mask used for this etch step) hole-dopes graphene; this occurs because the structure of HSQ becomes oxygen-rich with increased exposure [57]. Using a reactive ion etch (RIE) tool, an argon plasma etch recipe is developed. Before the graphene etch step, a sample coated with ZEP520 resist is used to calibrate the etch rate.

2.4 Epitaxial Graphene

Carriers in epitaxial graphene generally exhibit lower mobilities since they scatter off grain boundaries formed during the growth process. As a result, exfoliated graphene is preferred for most of the work of this thesis. (For exfoliated graphene, the graphene lattice within a single flake is single-crystalline, and devices are patterned out of a single

flake). However, epitaxial graphene has a clear advantage over exfoliated graphene: its method of graphene synthesis is more amenable to large-scale manufacturing. When differences in the two platforms lead to key differences in device characteristics, those differences in epitaxial graphene are explored (see the discussion on substrate-induced variation in epitaxial graphene in Section 5.4). Ultimately, the realization of graphene electronics must bring together the work of both platforms.

The "graphitization" process for epitaxial graphene involves the sublimation of Si from semi-insulating SiC and the subsequent rearranging of carbon atoms into graphene [58]. The work of this thesis uses epitaxial graphene on the Si-terminated face (0001) of 4H-SiC (Cree, Inc.) in a radio-frequency (RF) induction furnace. The fabrication process flow for epitaxial graphene devices builds upon the process flow for exfoliated graphene devices (Section 2.2). In epitaxial graphene, a gated device requires top-gate processing. Herein, e-beam evaporated SiO_2 is used as the gate dielectric and e-beam evaporated Ti/Au is used as the gate metal. The epitaxial graphene process flow for a three-terminal, top-gated device is shown in Figure 2.5.

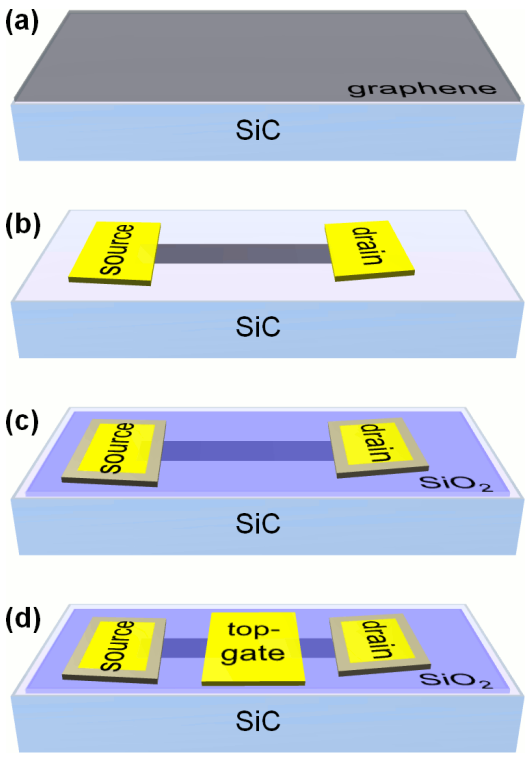

Figure 2.5: Epitaxial graphene fabrication process flow for a three-terminal, top-gated device. In (a), graphene is synthesized by sublimation of Si from a 4H-SiC(0001) substrate. In (b), EBL and metal liftoff are used to pattern contact electrodes (Ti/Au). A second EBL step and dry etch (via argon plasma) patterns the graphene device structure. In (c), a top-gate dielectric (SiO_2) is deposited via e-beam evaporation; a third EBL step and dry etch opens holes to the contact electrodes. The resist mask is then removed using 1165. Note that the HSQ used as the resist mask in (b) is not removed, so that gate dielectric is composed of HSQ and SiO_2. Finally, in (d), a fourth EBL step and metal liftoff are used to align top-gate electrodes (Ti/Au) to the graphene device.

2.5 Electrical Characterization

Four-point probe measurements are performed with standard lock-in techniques using an SRS-830 lock-in amplifier. An HP4156 semiconductor analyzer or Keithley 2612 source meter is used for pulsed gating. In general, for exfoliated graphene, back-gate biasing ranges from –100 V to +100 V for a 300 nm oxide dielectric and from –30 V to +30 V for a 90 nm oxide dielectric. This is to ensure that the oxide dielectric does not prematurely break down. A Cascade Microtech probe station is used for testing at room-

temperature under ambient exposure while a Lakeshore cryostat is used for testing at either room-temperature or cryogenic temperatures (down to T = 77 K by cooling with liquid nitrogen) under high-vacuum (~10^{-5} Torr). Figure 2.6 shows σ-V_{gs} measurement for a three-terminal, back-gated graphene device. The difference between the applied gate voltage (V_{gs}) and the gate voltage at the minimum conductivity point ($V_{g,min}$) determines the carrier density, according to:

$$n = \frac{C \cdot (V_{gs} - V_{g,\min})}{e} \tag{2.1}$$

where n is induced carrier density, C is capacitance per unit area formed between the graphene device structure and the gate structure, and e is elementary charge. In exfoliated graphene, a relatively thick gate oxide (90 or 300 nm) results in large fringe fields for ultra-narrow graphene devices ($W \leq 100$ nm) and the capacitance used in Equation (2.1) increases beyond its parallel-plate estimate. A discussion of the fringe effect is reserved for Chapter 4, where mobility is extracted for ultra-narrow devices. In Figure 2.6, the hallmarks for a clean, high-quality graphene are observed: high conductance, symmetric and linear behavior around the minimum conductivity point, and a decent on-off ratio. The ambipolar nature of carrier transport (i.e., electrons and holes both contribute) is understood in terms of the symmetric bandstructure of graphene. At large negative gate voltages, E_F shifts deep into the valence band, and holes are the majority carrier. At large positive gate voltages, E_F shifts deep into the conduction band, and electrons are the majority carrier. Tuning of E_F to the Dirac point (i.e., $V_{gs} = V_{g,min}$, where the conduction and valence bands meet) corresponds to the minimum conductivity point. It should also be noted that the σ-V_{gs} data were taken with the device exposed to atmosphere. In this environment, $V_{g,min}$ shifts to the right (i.e., to more positive gate voltages) with increasing

exposure, indicative of hole-doping of graphene (this effect is discussed in the context of device variation in Chapter 5). A two-step protocol is thus used to clean the devices before testing. First, the probe station chuck is heated to ~150 ˚C to bake off adsorbates on the graphene surface. Second, vacuum desorption helps pump away remaining adsorbates (the pressure inside the probe station reaches ~10^{-5} Torr).

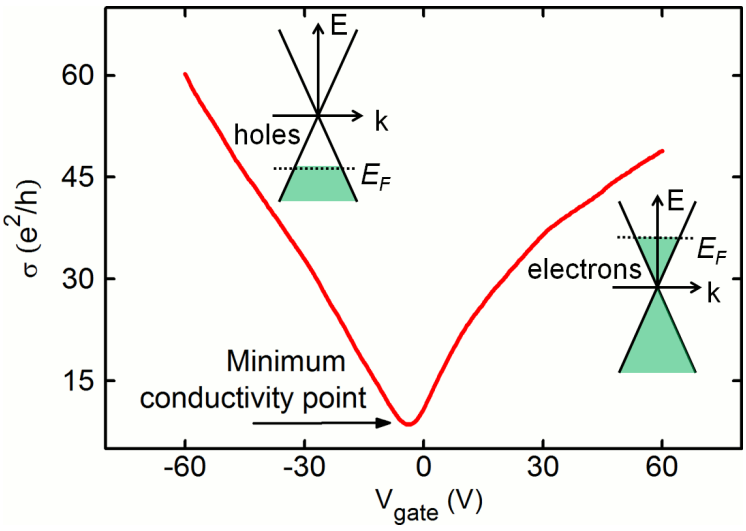

Figure 2.6: σ-V_{gate} behavior of a high-quality, three-terminal graphene device. A high conductance and symmetric, linear behavior around the minimum conductivity point, and a decent on-off ratio are observed.

2.6 Structural Characterization

Atomic force microscopy (AFM), Raman spectroscopy, and scanning electron microscopy (SEM) function as key metrology tools during the fabrication process and provide structural data to complement electrical testing. SEM and AFM reveal structural information of as-synthesized graphene or patterned graphene devices. AFM and Raman indicate the number of layers. In addition, the D-band of graphene in Raman analysis reveals its defect density while the shift of the G- and 2D-bands reveals the type and extent of doping. Using these tools, structural characterization helps verify whether a

particular process step introduces defects into graphene. Figure 2.7 shows SEM images of various device structures used in this work. In Figure 2.7a, the device was imaged after patterning of HSQ but before the plasma etch step (thus the outline of the flake remains visible); all other devices shown here were imaged after the plasma etch step.

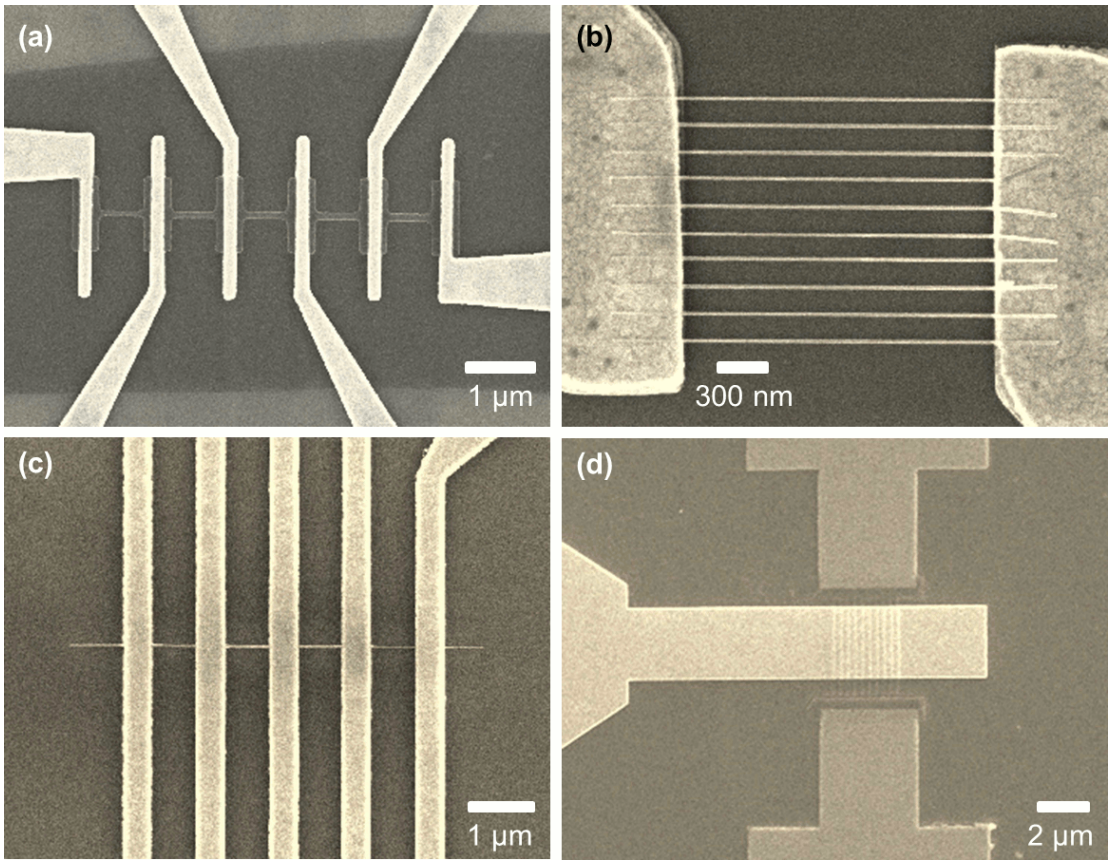

Figure 2.7: SEM images of various device structures: a 200 nm wide graphene ribbon with selective p- and n- doping along the length of the ribbon (a), a two-point testing configuration for a device with a set of ten parallel GNRs (b), a four-point testing configuration for a device with a single GNR (c), and a top-gated epitaxial graphene device with a set of ten parallel GNRs (d).

2.7 Conclusion

A work flow, which comprises design, fabrication, and electrical and structural testing, is developed and qualified for exfoliated graphene devices. Process integration

helps minimize contamination throughout the fabrication process, and includes sample cleaning before exfoliation, layout considerations for contact electrodes, and plasma etch tuning. These process integration methods, in combination with high-resolution e-beam lithography, deliver the manufacture of high-quality, nanoscale graphene devices. For epitaxial graphene, this fabrication process flow is modified by the addition of a top-gate process (gate dielectric and metal stack) to permit top-gating. It is additionally used as the baseline process flow in the manufacture of graphene p-n junction devices in Chapter 6. Electrical testing via standard lock-in techniques is used to characterize device behavior. AFM, SEM, and Raman analyses uncover the quality and composition of as-synthesized graphene or patterned graphene devices. Together, these tools are an integral part of the metrology testbed for the fabrication process and also help supplement electrical testing results.

CHAPTER 3

CURRENT-CARRYING CAPACITY AND THERMAL MANAGEMENT IN GRAPHENE DEVICES

3.1 Introduction

Graphene is a promising material for electronics because of many interesting properties including high intrinsic mobility, atomic flatness, and a width-dependent bandgap. That graphene is a single layer eliminates thickness variation and mitigates short-channel effects that hamper deep sub-μm silicon technology. A greater current-carrying capacity permits greater device reliability and performance at higher operating voltages and currents. Electromigration is a current-assisted diffusion process that limits the current-carrying capacity of a wire; for very narrow wires, this process can lead to voids and cause electrical failure. In metals, this current-carrying capacity is approx. 10 nA/nm^2. Thus in the context of interconnects, a greater current-carrying capacity allows miniaturization of graphene wires. Many studies have investigated breakdown current density in CNTs; by inducing electrical breakdown, current-carrying capacity in single- [59] and multi-walled [60] CNTs is found to be on the order of 10 $\mu A/nm^2$. In carbon nanofibers, J_{BR} is found to be on the order of 10 nA/nm^2 [61, 62]. As a result of strong sigma bonds formed between carbon atoms, estimates suggest that J_{BR} of graphene should be on the same order as for CNTs. However, little experimental evidence existed on the electrical breakdown of either large-area graphene or graphene nanoribbons. Suspended graphene (in 2D, large-area form) has been shown to have a high thermal

conductivity (k) as high as 5000 W/m-K [26]. This helps keep graphene devices cool, further improving reliability. In the present study, it is experimentally shown that graphene nanoribbons demonstrate an impressive breakdown current density (J_{BR}) and thermal conductivity (k).

3.2 Experimental Methods—Inducing Electrical Breakdown

Exfoliated graphene (1–5 layers; from Kish graphite) is prepared on a supporting SiO_2 substrate. E-beam lithography is used to pattern the contact electrodes and graphene devices. Each device consists of ten parallel graphene nanoribbons; widths for all GNRs within a device are designed to be the same. The range of widths studied is 16 nm < W < 52 nm, while the range of lengths is 0.2 μm < L < 0.75 μm. This particular device layout (a set of ten identical GNRs) increases the density of ribbons per flake and thus makes them more robust to variation (such as the variation in impurity density from ribbon to ribbon). As a result, this device configuration is generally used throughout this thesis for the study of nanoscale graphene. To investigate current-carrying capacity, a voltage ramp is applied to the device. With increasing current density, there is a voltage at which the first GNR (within the set of ten) breaks down, resulting in a visible drop in current. This breakdown technique has been used to study current and voltage limits in CNTs [59, 60] and carbon nanofibers [61, 62]. Electrical breakdown has also been used to burn away successive shells in a multiwall CNT [63, 64] or to obtain semiconducting CNTs from a mixture of CNTs (since metallic ones burn away at a lower voltage) [65]. In this study, the bias cycling from 0 V until the next breakdown event is repeated until all GNRs of the device break down.

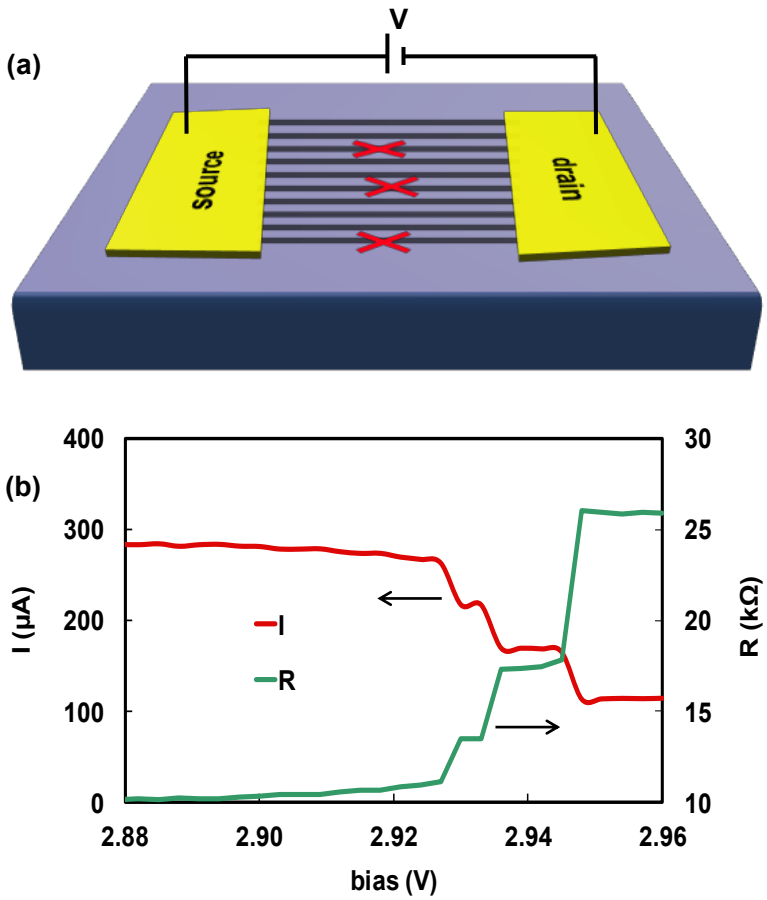

Figure 3.1: Method for electrical breakdown of graphene ribbons. A voltage ramp is applied between source and drain electrodes until a breakdown event occurs (a). The corresponding I-V for three successive breakdown events is shown in (b).

To test for breakdown more reliably, the ramp voltage is re-started after each breakdown event (with a hold time of 3 min. between each ramp test) to minimize self-heating effects of graphene. This resulted in the breakdown of a device one ribbon at a time (instead of having multiple ribbons break down simultaneously). The resistance of each ribbon is extracted from the difference in conductance immediately before and after a breakdown event. J_{BR} is then found from the resistance and breakdown voltage (V_{BR}) of the GNR. Figure 3.2 shows the current-voltage (I-V) behavior of a device with ten GNRs in parallel taken through electrical breakdown—the top I-V curve is for all ten GNRs, the

second I-V curve from the top is for the remaining nine GNRs, and so forth. Each I-V is initially linear and becomes saturated at increasing bias. This saturation is repeatable as the device is cycled from 0 V to 2 V. Contact resistance is found to be unchanged after bias cycling, suggesting that the resistance increase at high bias is due to self-heating effects and not due to contact annealing. Such I-V saturation has been observed at high bias [60] in CNTs. Of the 21 devices tested in this study, 14 showed a ~2X increase in resistance (that is, resistance near the breakdown voltage compared to resistance at low bias), 6 showed a 10–20% increase, and one device showed no increase. The reason for this varying behavior could be two-fold: (i) a higher impurity density (n_{imp}) causes an earlier onset of current saturation as a result of increased electron-phonon scattering [66]; n_{imp} varies in the range $2–19\times10^{11}$ cm^{-2} for the devices in this study; (ii) ballistic transport in short-length devices; it has been argued [67] that ballistic transport (in CNTs) results in a linear I-V behavior with no current saturation at high bias. From repeated low-bias measurements (V_{ds} = 10 mV) immediately after a breakdown event, it is found that 2–3 min. are needed for a device to return from a self-heated state to a stable state. Thus, low-bias measurements reported in this work are done 3 min. after any previous high-bias cycling. The contact resistance is found to be almost constant after each event and is in the range of 30–80 Ω for the devices in this study. With a contact area of 0.5–1 μm^2, this translates to a contact resistance of 15–80 $\Omega\cdot\mu m^2$. The breakdown voltage V_{BR} is seen to be around the same for all the ten GNRs in this device. Occasionally, it is seen that V_{BR} of a later breakdown event is smaller than that of the previous event. This may occur if the device has not fully reached its stable state from the previous high-current cycle. The inset to Figure 3.2 shows the breakdown current density of the ten GNRs, extracted by

comparing current levels before and after breakdown. For this device, the range of J_{BR} is between 1.2 and 2.8 μA/nm^2. The observed variation across individual ribbons could be because of a variation in impurity density.

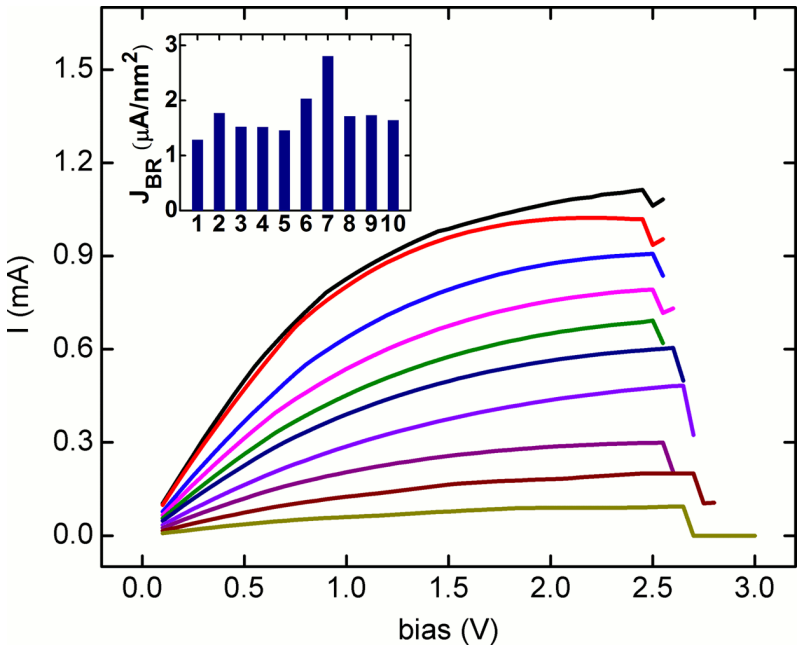

Figure 3.2: I-V curves of ten identical GNRs taken through electrical breakdown. Each GNR has a width of 22 nm and a length of 0.75 μm. The inset shows that these GNRs have a breakdown current density in the range of 1.2–2.8 μA/nm^2.

3.3 Current-Carrying Capacity

These experiments were repeated across 21 devices with GNR widths in the range of 16–52 nm. Interestingly, breakdown occurred at nearly a constant voltage across all devices (in the range of 2.5–3 V), anticipating an inverse relation between J_{BR} and ρ. Figure 3.3a shows breakdown current density for over 100 GNRs vs. their low-bias resistivity (taken at V_{ds} = 10 mV). Using this testing method, J_{BR} is found to be between 0.26 and 22 μA/nm^2; this corresponds to a power density between 0.65 and 55 μW/nm^2. The best fit for this low-bias testing data is obtained via $J_{BR} = A \cdot \rho^{-B}$, where A = 57.2

μA/nm^2, and B = 0.71, with ρ in units of μΩ-cm; R^2 for this fit is 74%. In this analysis, however, note that J_{BR} is extracted when the GNR is self-heated; low-bias resistivity of a GNR, on the other hand, is extracted from the conductance difference between low-bias measurements done before and after a breakdown event. Figure 3.3b shows J_{BR} vs. high-bias resistivity, extracted from the conductance difference before and after a breakdown event (i.e., for V_{ds} in the range of 2.5–3 V. For devices measured under high-bias testing, J_{BR} is found to be between 0.04 and 22 μA/nm^2; this corresponds to a power density between 0.1 and 55 μW/nm^2 The best fit for this high-bias testing data is obtained via $J_{BR} = A \cdot \rho^{-B}$ with A = 95.7 μA/nm^2 and B = 0.71; R^2 for this fit is 86%. Using the 1D heat transport equation, a relation of the type $J_{BR} \propto 1/\sqrt{\rho}$ has been proposed [62]. The exponent of 0.71 extracted from the data points to a faster breakdown with increasing device resistivity. This indicates that the same factors that cause a higher resistivity also cause degradation in breakdown current density, e.g. in-plane defects. For longer lengths, a relation of the type $J_{BR} \propto 1/\sqrt{(a\rho)}$ has been proposed [61], where a is cross-sectional area. Using a subset of data from Figure 3.3b that have $L > 0.5$ μm, a fit (not shown) via the relation $J_{BR} = A \cdot (a\rho)^{-B}$ with B = 0.55 is obtained; the fit has an R^2 of 92%. Finally, it should be noted that these break down events were measured with the graphene devices exposed to air. The study by Collins *et. al*. [60] posited that oxidation assists in the breakdown of multi-walled CNTs, suggesting that a greater current-carrying limit in graphene ribbons would be seen if the devices were encapsulated or tested in vacuum.

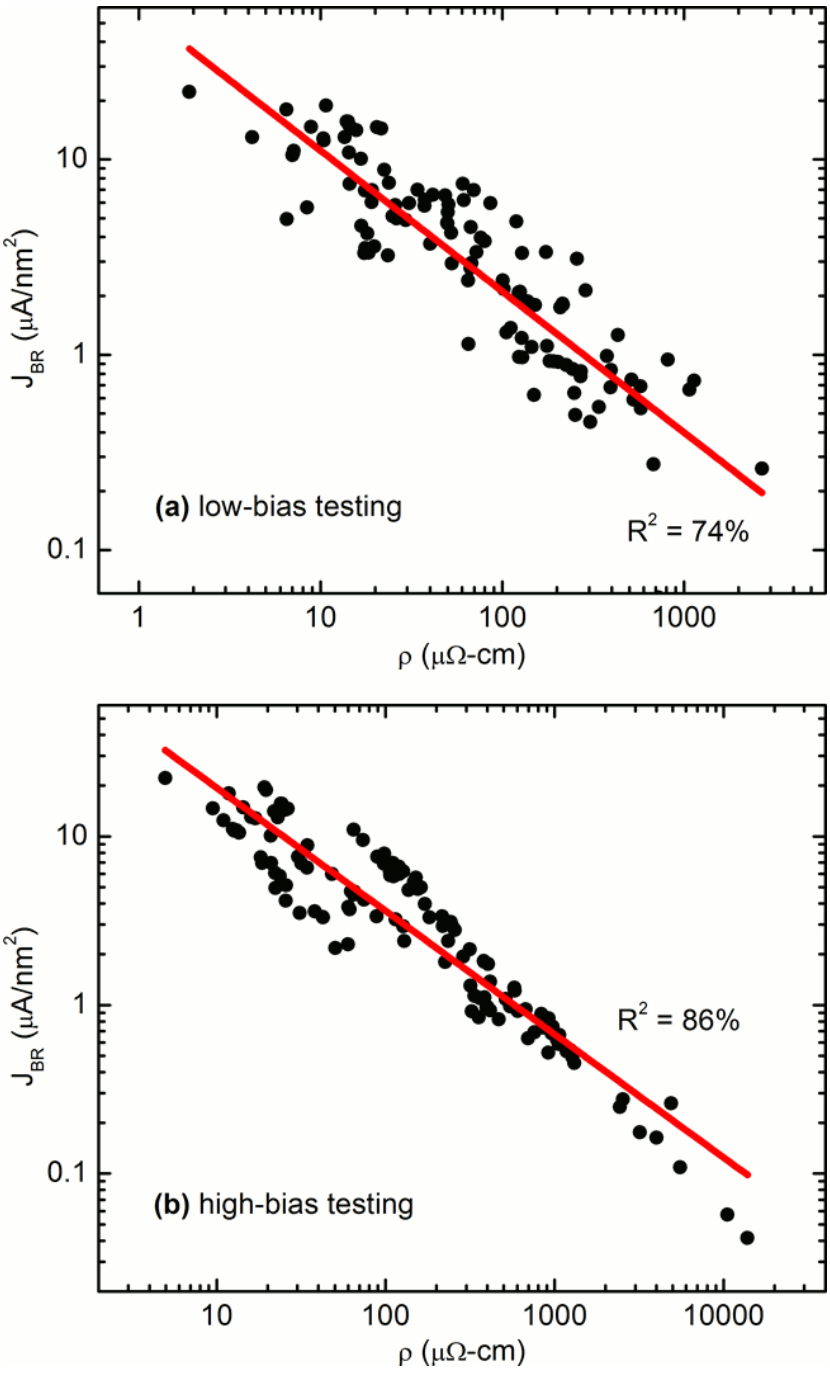

Figure 3.3: Breakdown current density vs. resistivity under (a) low-bias testing (R^2 for this fit is 74%) and (b) high-bias testing (R^2 for this fit is 86%). The fit for both plots is of the form $J_{BR} = A \cdot \rho^{-B}$ where $B = 0.71$. If the breakdown mechanism was Joule heating, theory predicts that the exponent in the fit should be 0.5; a steeper exponent in the fit indicates that the breakdown occurs faster for higher-resistivity GNRs, and might be indicative of higher defect densities contributing to faster electrical breakdown.

3.4 Thermal Conductivity

From SEM imaging, it was clear that breakdown occurred near the middle of the ribbon; this points to Joule heating (i.e., resistive heating) in the ribbon. Thus the likely breakdown mechanism is oxidation of graphene through Joule heating. It is possible to estimate the peak temperature of the GNRs in these experiments by solving the 1D heat transport equation [68]:

$$V_{BR} \cdot I_{BR} \cdot \left(1 - \frac{1}{\cosh\left(L/(2 \cdot L_H)\right)}\right) = g \cdot L \cdot (T_{max} - T_0) \tag{3.1}$$

where V_{BR} and I_{BR} are breakdown voltage and current, respectively, L is GNR length, g is heat dissipation coefficient per unit length of the GNR to the substrate and top resist, T_{max} is peak temperature in the ribbon, and T_0 is the contact electrode temperature. Herein, L_H is the characteristic thermal healing length along the GNR and is given by $(ka/g)^{1/2}$, where k and a are thermal conductivity and cross-sectional area of the GNR, respectively. Since $V_{BR} \cdot I_{BR} = I_{BR}^2 \cdot R = (J_{BR} \cdot A)^2 \cdot (\rho \cdot L/A)$, Equation (3.1) can be rewritten as:

$$g(T_{max} - T_0) = J_{BR}^2 \cdot \rho \cdot A \left(1 - \frac{1}{\cosh\left(L/(2 \cdot L_H)\right)}\right) \tag{3.2}$$

For a representative GNR (selected from Figure 3.3), J_{BR} = 3.6 μA/nm^2 and ρ =38 μΩ-cm. To evaluate T_{max}, it is necessary to assume values for g, T_0 and T_{max}. Through finite element analysis in a previous study [69], g was found to be around 1 W/m-K for sub-100 nm wide GNRs on SiO_2. T_0 is assumed to be at room temperature since metal contacts act as good heat sinks for graphene devices [70]. It has been reported [71] that the peak temperature in the middle of μm-wide SLG on SiO_2 is at least 500 °C. This result is consistent with the fact that oxidation of graphene in ambient air occurs at ~600 °C [72], which induces electrical breakdown. Thus, k is used as a fit parameter to obtain realistic

values of T_{max}. For k = 205 W/m-K, g = 1 W/m-K results in a T_{max} (i.e., temperature at breakdown of GNR) of 600 °C. It should be noted that this thermal model assumes that heat dissipation of the GNR along its length is small compared to that through the SiO_2 substrate. The thermal conductivity thus extracted—204 W/m-K—is for a 22 nm wide GNR. Similar calculations result in a thermal conductivity in the range of 30–800 W/m-K for the GNRs in this study. By comparison, recall that large-area (μm-wide), suspended graphene yielded k upward of 5000 W/m-K at room temperature [26]. Edge scattering in graphene ribbons has been argued to result in a size-dependent thermal conductivity [73]; k at room temperature is found to reduce from 5500 to 3000 W/m-K as GNR width is scaled from 9 to 3 μm. In addition, umklapp scattering, a phonon scattering process that dominates thermal conductivity at high temperatures, reduces k as temperature increases beyond 100 K [73]. Since the GNRs under discussion are both narrow and self-heated, it is expected that both edge scattering and umklapp scattering play an important role in determining k.

3.5 Conclusion

The impressive current-carry capacity and thermal conductivity of sub-100 nm wide GNRs is studied using electrical breakdown [74]. J_{BR} is found to have a reciprocal relation with ρ (an indication of device quality). While the majority of devices exhibit a J_{BR} between 0.1 and 10 μA/nm^2, high-quality devices exhibit a J_{BR} of ~10 μA/nm^2 and resistivity of ~10 μΩ-cm. A representative high-quality, single-layer graphene ribbon with W = 30 nm and L = 200 nm exhibits a current limit of ~100 μA, breakdown electric field of ~100 kV/cm, and breakdown power of 200 μW. In addition, these ribbons

demonstrate a thermal conductivity in the range of 30–800 W/m-K. Thus although the *k* of GNRs is reduced from its intrinsic value of 5000 W/m-K (in suspended graphene), high-quality devices nevertheless demonstrate an excellent ability to conduct heat. These findings have two benefits for graphene as an electronic material. First, a high current-carrying capacity permits more robust device operation at higher voltage and current levels. This, combined with the fact that graphene is atomically thin, suggests that graphene devices could be less sensitive to short-channel effects. Second, a high thermal conductivity assists in the thermal management of graphene devices. A cooler chip improves performance and reliability, and contributes to a reduced power consumption. Additionally, the electrical breakdown technique can be used to manage variation: in a device configured with parallel ribbons, ribbons that are more metallic dissipate greater power and can be burned off.

CHAPTER 4

SIZE EFFECT IN NANOSCALE GRAPHENE

4.1 Introduction

The scaling of graphene from 2D, large-area form to 1D, graphene nanoribbon form opens a semiconducting bandgap. In any low-dimensional system, confinement of charge carriers gives discretized energy levels [75]; in graphene, this phenomenon opens a gap between the conduction and valence bands. Further, the study of GNR transport gives insight into 1D transport properties such as the relative importance of edge states and the crossover from 2D to 1D transport, where localization effects take hold. The study of transport in 1D graphene is thus relevant from both a practical and fundamental scientific point of view.

As the dimensions of a material are scaled, significant changes occur in carrier transport: carrier quantization alters the charge distribution and edge/boundary scattering degrades mobility. Two principle factors should be considered in the use of graphene nanoribbons as a platform for field-effect transistors. First, ideal GNRs with atomically smooth edges witness a decrease in mobility with scaling, a consequence of the inverse relation of bandgap and mobility. A study by Obradovic *et al.* [76] revealed that lattice phonons in sub-5 nm wide GNRs (modeled with no edge disorder and decoupled from a substrate) degrade mobility to values below 1×10^4 $cm^2/V\text{-}s$. Second, realistic GNRs with rough edges experience edge scattering that further degrades mobility. For these GNRs, either lithographically patterned or chemically produced, a certain quantity of LER

results from the fabrication process. Carriers in GNRs thus undergo diffusive scattering at the edges rather than specular scattering, Figure 4.1. A number of theoretical studies have quantified the impact of LER-induced scattering on carrier transport in graphene nanoribbons. In [77], for a moderately disordered armchair-GNR FET with $W = 4.18$ nm, I_{on}/I_{off} for the device is degraded by more than a factor of 10 from that of an ideal GNR with perfect edges. In a study by Fang *et. al*. [78], various scattering mechanisms and their impact on carrier transport are modeled; it is predicted that the onset of LER-limited mobility occurs for GNRs with $W < 4$ nm (assuming an edge roughness amplitude of 0.5 nm). On the experimental side, numerous studies have measured mobility in graphene but most of these have been on wide ribbons ($W > 1$ μm). Narrow GNR characterization has been in the context of bandgap opening. This work provides the first experimental study of the size effect in nanoscale graphene. Finally, potential methods to mitigate the size effect are discussed.

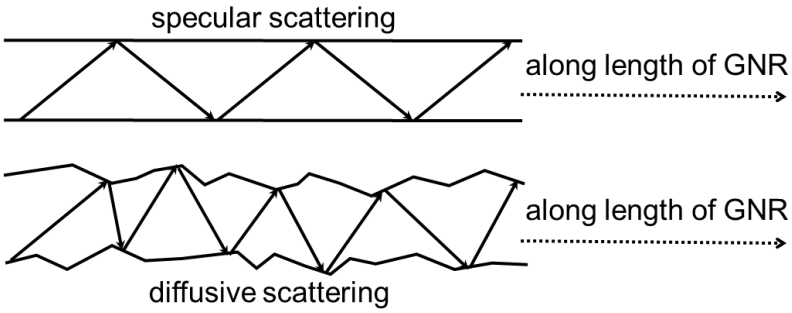

Figure 4.1: Specular vs. diffusive scattering. In specular scattering (top), carriers scatter off smooth edges without any loss in momentum in the direction of propagation. In diffusive scattering (bottom), carriers scatter off rough edges with a loss in momentum.

4.2 Characterization of Line Edge Roughness

For the devices in this study, line-edge roughness of graphene ribbons is induced in the fabrication process—during e-beam lithography and the subsequent plasma etch

step. The EBL step that defines the mask (to etch graphene) uses HSQ resist. After e-beam exposure, the unexposed HSQ regions are removed using microposit MF-319 developer (Shipley Company), leaving a certain amount of line-edge roughness in the remaining HSQ ribbon structures. SEM imaging reveals that LER for these HSQ ribbons is around 2–3 nm and is independent of ribbon width, Figure 4.2. (LER is defined as the root mean square of the spacing between the actual edge and the ideal edge that would be formed by a straight line connecting the endpoints of the edge of a ribbon.) The amount of LER in the HSQ structures is assumed to be faithfully reproduced in the underlying graphene sheet upon plasma etching. This is a reasonable assumption because graphene is atomically thin, making it difficult for the plasma to laterally etch the graphene sheet underneath the HSQ structures. With a C-C bond length (a_0) of just 0.14 nm in graphene, the edges of the patterned graphene ribbons are clearly very rough on the atomic scale. It should also be noted that the extent of LER seen in these ribbons neutralizes any dependence on edge configuration. In ideal ribbons (without any edge roughness), edges exhibit a zigzag or armchair configuration. In realistic ribbons (with some edge roughness), edges exhibit some mixture of the two configurations, and differences in transport of GNRs with zigzag edges and GNRs with armchair edges are washed out. As a result, the impact of the size effect can properly be attributed to LER rather than the confounding influence of both LER and edge configuration.

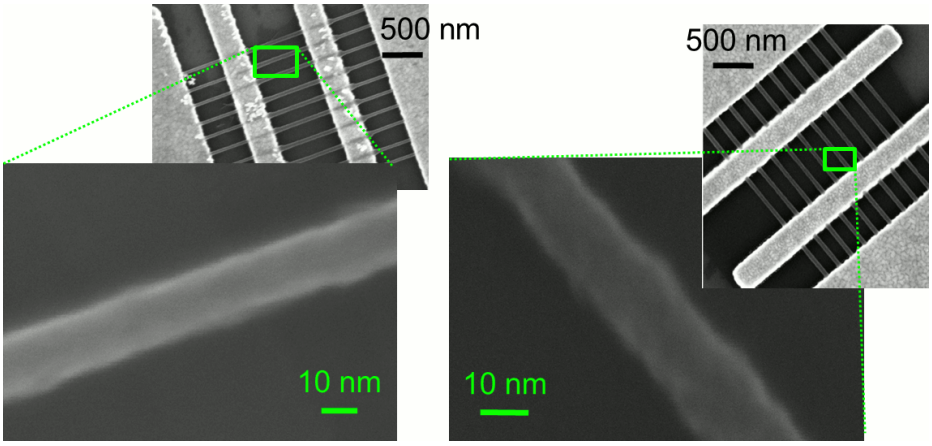

Figure 4.2: SEM characterization of line edge roughness in GNRs. The HSQ/graphene structures exhibit line-edge roughness of around 2–3 nm, independent of ribbon width. Herein, LER is defined as the root mean square of the spacing between the actual edge and the ideal edge that would be formed by a straight line connecting the endpoints of the edge of a ribbon

4.3 Experimental Methods—Extracting the Size Effect

To characterize the impact of edges roughness on carrier transport in graphene devices, mobility is compared across a range of GNR widths. The mobility of these (1D) graphene nanoribbons is compared to the mobility of (2D) large-area graphene before ribbon patterning. In large-area graphene, there are three primary scattering sources—lattice phonons, remote phonons from the SiO_2 substrate, and impurities at the graphene-substrate interface. In typical devices, impurity scattering dominates over remote phonon scattering, which in turn dominates over lattice phonon scattering. So, total mobility in large-area graphene is determined by impurities. In graphene nanoribbons, there is an additional scattering source—edge defects from LER. By measuring the difference in the total large-area mobility before the plasma etch step and the total GNR mobility after the plasma etch step, the electrical impact of the size effect on GNR transport is extracted. (It is assumed here that the plasma etch step does not contribute to a degradation of mobility

either by defect generation in graphene or by some other mechanism. This assumption has been verified by sequentially etching various devices; after the initial decrease due to etching of graphene, no further decrease in mobility is seen over long periods of plasma etch. This is reasonable to expect since graphene that remains after the etch step is protected by HSQ resist.)

Mobiliy is found using one of two ways. In one method, mobility is extracted via $\mu = \sigma/(n \cdot e)$, where σ is drain conductance of the device measured at a specified carrier density n (given by Equation (2.1)). This is the effective mobility. In another method, mobility is extracted via $\mu = g_m/(C_{ox} \cdot W/L \cdot V_{ds})$ where g_m is transconductance of the device measured at a specified carrier density n. This is the field-effect mobility. For graphene, field-effect mobility is lower than effective mobility because of a non-linear I_{ds}-V_{gs}. Only when I_{ds}-V_{gs} is linear does field-effect mobility equal effective mobility. To compare the two methods, σ and g_m should be extracted at the same carrier density n, given that the device is operating in a linear I_{ds}-V_{gs} region at this carrier density. This assumption holds for n in the range of $2–5\times10^{12}$ cm^{-2}, where n is large compared to impurity density. At any rate, for high-quality devices, the difference is small, and it is found that overall data trends hold irrespective of which method is used. Thus, for consistency, in the present study and in the rest of the thesis, effective mobility is used.

Another key factor in extracting mobility is the fringe effect on capacitance—the additional capacitance between conductive structures that arise from electric fields that extend some distance away from the region directly between the structures. This effect is simulated using COMSOL Multiphysics (a finite element analysis / simulation software) with GNRs modeled as strip capacitors, Figure 4.3a-b. Each device is modeled as a set of

ten parallel GNRs on a 300 nm SiO_2 dielectric ($\mathcal{E}_r$ = 3.9) atop a silicon substrate; each ribbon is 1 nm thick and 400 nm long. The ribbon-to-ribbon pitch is fixed at 200 nm while ribbon width is varied (according to the range of fabricated devices of this study). The simulation uses a coarse mesh with 70 V applied to the silicon substrate and the GNRs grounded (to reproduce typical testing conditions). The fringe factor—the total capacitance of a GNR (with fringe fields) normalized to its ideal parallel-plate capacitance (without fringe fields)—is shown vs. ribbon width in Figure 4.3c for the device with ten parallel ribbons, as well as for a single, isolated GNR. While all devices herein are designed to have ten parallel ribbons, some devices contain less than ten ribbons after processing as some ribbons are lost to misalignment or other yield-related fabrication issues. Figure 4.3c thus shows the fringe factor for both a structure with ten parallel ribbons and a structure with a single GNR. The capacitance per unit area of a single GNR is 40–50% higher than that of ten parallel GNRs. This result is expected since adjacent ribbons partially block out fringe fields. The device with the narrowest ribbons in this study (W = 16 nm) has a fringe factor of 10. In regards to the mobility calculation, the fringe factor renormalizes V_{gs}–$V_{g,min}$ at a specified carrier density (since the assumed capacitance of the device changes).

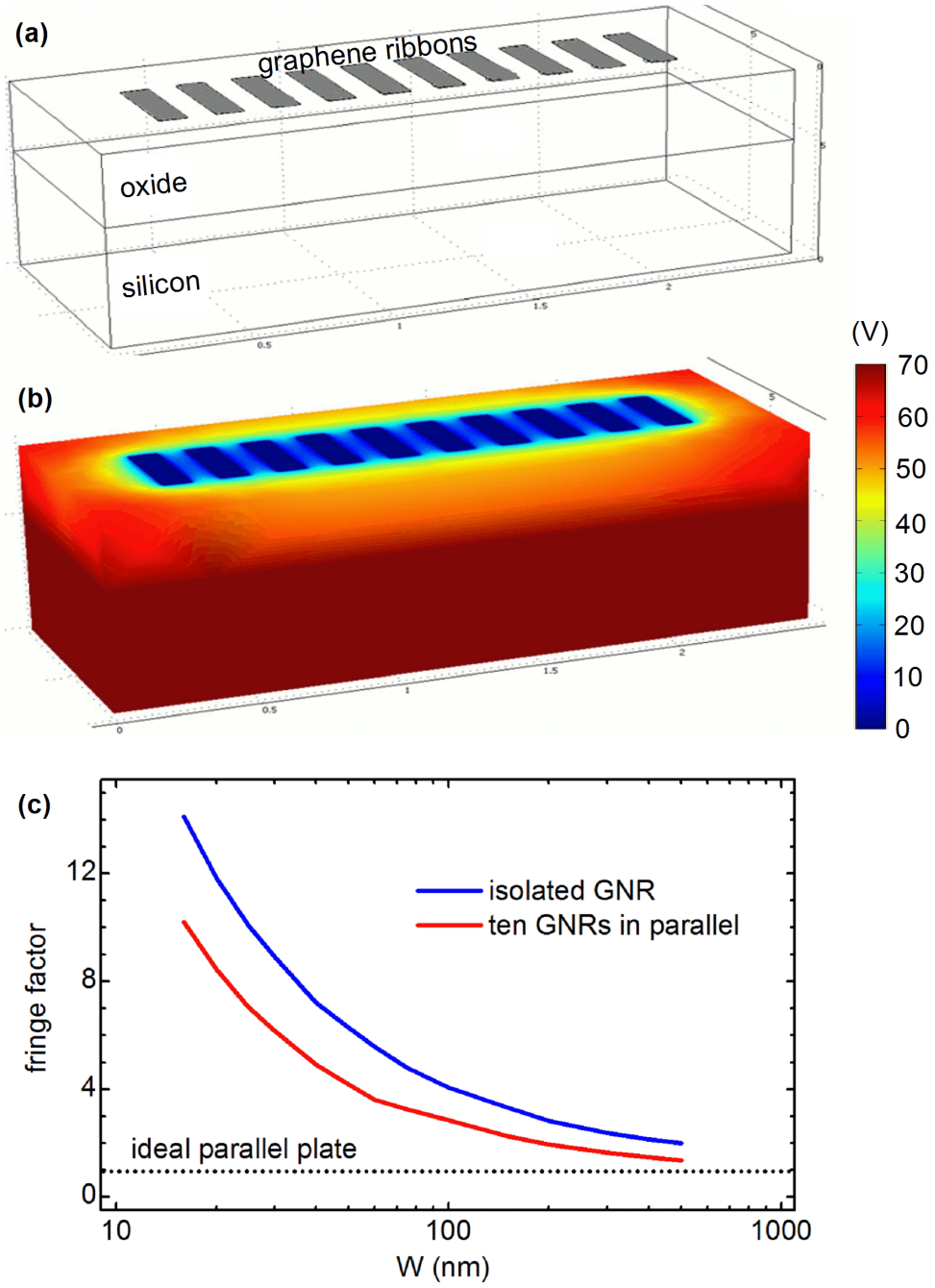

Figure 4.3: Fringe effect for GNRs on a SiO_2/silicon substrate. In (a), the setup of the capacitance simulation via COMSOL is shown—a set of ten parallel GNRs, each 1 nm thick and 400 nm long on a 300 nm SiO_2 dielectric ($\mathcal{E}_r$ = 3.9) atop a silicon substrate. Ribbon width is varied according to the range used in this study (the ribbons in this particular schematic have W = 100 nm). In (b), simulated voltages across the structure are shown, using a coarse mesh with 70 V applied to the substrate and the GNRs grounded. The fringe factor—the capacitance of a GNR normalized to its ideal parallel-plate capacitance—is shown vs. ribbon width in (c) for the device (with ten parallel ribbons), as well as for a single, isolated GNR.

Exfoliated graphene (1–8 layers; from Kish graphite) is prepared onto a 300 nm thick SiO_2 film atop a doped Si substrate. GNRs with widths in the range 16 nm < W < 1000 nm are patterned. LER of these ribbons, extracted by SEM imaging, is found in the range of 2–3 nm, independent of ribbon width. An SEM image of four devices (across five electrodes) is shown in Figure 4.4. For the devices in this size effect study, a single device is considered to be a set of ten parallel GNRs (rather than a single, isolated GNR). The four devices in Figure 4.4 (as is the case for any set of four devices in this study) are patterned out of the same flake as this helps minimize device-to-device variation.

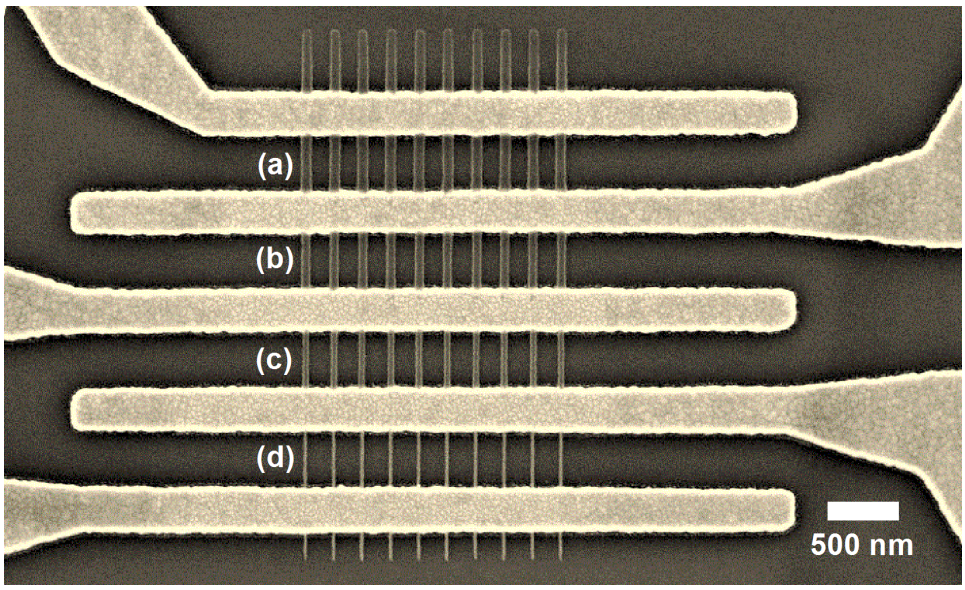

Figure 4.4: SEM image of four devices after the plasma etch step. A a single device is a set of ten parallel GNRs (vertical lines in image) between an electrode pair (horizontal fingers in image). The GNRs (covered by HSQ in the image) are (a) 68 nm, (b) 58 nm, (c) 42 nm, and (d) 20 nm wide with a ribbon-to-ribbon pitch of 200 nm; all have a length of 400 nm.

4.4 Interplay of Edge, Impurity, and Remote Phonon Scattering

In exfoliated graphene, impurity scattering results from impurities trapped at the graphene/SiO_2 interface. How do these impurities impact mobility? Impurity-limited

mobility (μ_{imp}) is estimated [79] to have a reciprocal relation with n_{imp}; that is, $\mu_{imp} = 4.8\times10^{15}\cdot(1/n_{imp})$ 1/V–s. Overall, devices in this study have n_{imp} in the range of 1.1×10^{11}–2.2×10^{12} cm^{-2}, corresponding to μ_{imp} in the range of 4.4×10^{4}–2,200 cm^2/V-s. To isolate the impact of edge disorder (by minimizing any variation caused by impurity scattering), it is better to compare devices with a similar n_{imp}. Thus, for the plot of GNR mobility vs. ribbon width shown in Figure 4.5, devices have n_{imp} in the range of $1–2\times10^{12}$ cm^{-2}, corresponding to μ_{imp} in the range of $2–4\times10^{3}$ cm^2/V-s. It is seen that above a threshold width (at around 50 nm), total GNR mobility is independent of width; for wider ribbons, substrate impurities dominate carrier transport (yellow band in data plot). On the other hand, below this threshold width, total GNR mobility is seen to decrease sharply. This is the manifestation of the size effect—where edge scattering begins to dominate carrier transport (blue band in data plot). This behavior is also independent of the thickness of graphene. GNR mobility is seen to decrease from around 3000 cm^2/V-s for W = 100 nm to less than 200 cm^2/V-s for W < 20 nm. Mobility in GNRs is thus limited by the interplay between edge scattering and impurity scattering.

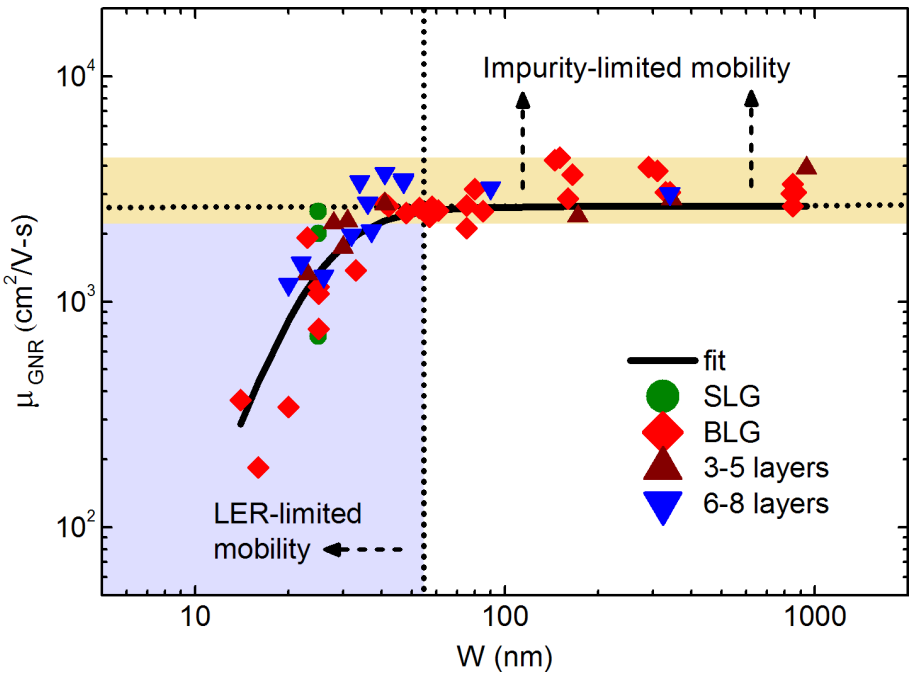

Figure 4.5: Size effect in nanoscale graphene devices. Total GNR mobility (μ_{GNR}) is plotted vs. ribbon width for 54 devices of varying thickness: single-layer (SLG), bi-layer (BLG), 3–5 layers, and 6–8 layers. For $W < 50$ nm, mobility is limited by edge scattering; for $W > 50$ nm, mobility is limited by impurity scattering.

A first-order model for GNR mobility is derived by accounting for the following scattering sources: (i) intrinsic lattice phonon scattering that limits mobility to 2×10^5 cm^2/V-s ($\mu_{lattice}$), (ii) SiO_2 remote phonon scattering that limits mobility to 4×10^4 cm^2/V-s, (iii) impurity scattering, and (iv) LER-induced scattering (i.e., edge scattering). Using Matthiessen's rule, the total GNR mobility can be written as

$$\frac{1}{\mu_{GNR}} = \frac{1}{\mu_{lattice}} + \frac{1}{\mu_{SiO2}} + \frac{1}{\mu_{imp}} + \frac{1}{\mu_{LER}} \tag{4.1}$$

LER-limited mobility (μ_{LER})—determined by comparing device mobility before (large-area form) and after (GNR form) patterning—is seen to have a reciprocal relation with GNR width. The data fit, based on a least squares regression, is of the type $\mu_{LER} = A \cdot W^B$ where A = 0.001 cm^2/V-s, B = 4.3, and W is given in nm, Figure 4.6. This value of B

compares well with the result of $B = 4.0$ from Fang *et. al.* [78], where perturbation theory is used to calculate how LER alters the potential landscape near the ribbon edges (which induces carrier scattering). GNR mobility for $W > 50$ nm is seen to be limited by impurity scattering; at these widths, if impurity density is kept below 1×10^{11} cm^{-2}, mobility would be limited by SiO_2 phonon scattering. This is another way to view the size effect.

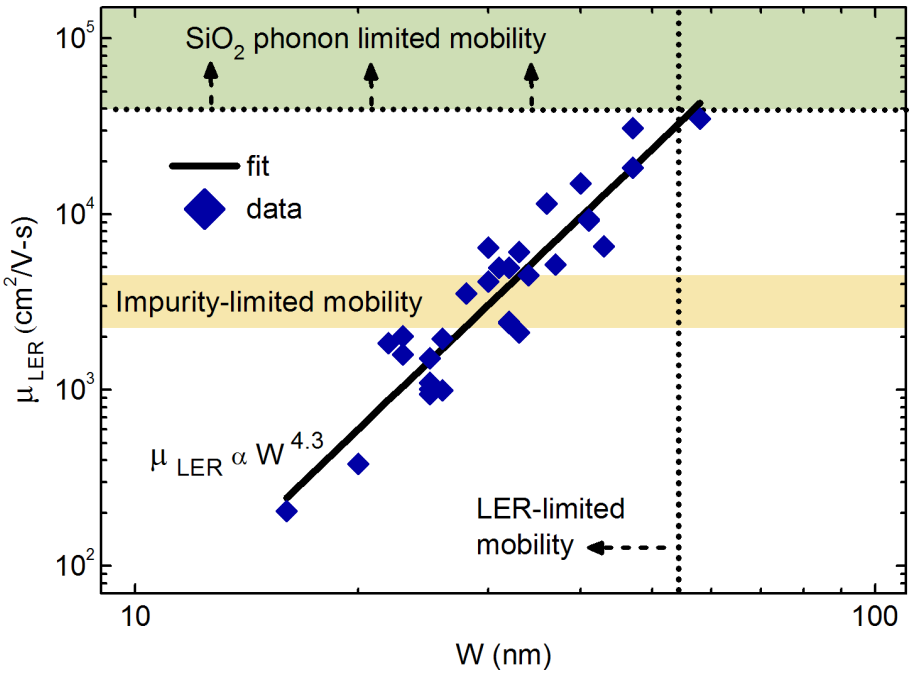

Figure 4.6: Interplay of edge scattering and remote phonon scattering in GNRs on a SiO_2 substrate. E-beam lithography and a plasma etch convert 2D, large-area graphene into 1D, graphene nanoribbons and thus introduce LER to the graphene devices. μ_{LER} vs. GNR width is extracted by comparing mobility of the device before and after the plasma etch step.

The fit for total GNR mobility plotted in Figure 4.5 is obtained by a least squares regression on Equation (4.1). The $\mu_{lattice}$ and μ_{SiO2} terms are neglected since μ_{imp} and μ_{LER} dominate carrier transport in GNRs. μ_{imp} is assumed to be 2700 cm^2/V-s (as an average value for the devices with n_{imp} in the range of $1–2\times10^{12}$ cm^{-2} while $\mu_{LER} = 0.001 \cdot W^{4.3}$. Note that since the narrowest GNR has a width of 16 nm, effective mass can be assumed

the same for the range of widths considered here. The impact of the size effect can thus be attributed to LER rather than any width-dependent effective mass.

4.5 Design Space for Graphene Nanoribbon FETs

This study presented the first experimental report on the electrical impact of the size effect in GNRs [80]. Edge-induced mobility degradation sets in at a ribbon width of ~50 nm. For W < 50 nm, edge defects limit GNR performance while for W > 50 nm, substrate impurities limit GNR performance. This onset of the size effect depends on both the extent of LER and impurity scattering in the devices. For smoother GNRs, this onset occurs at narrower widths. More pertinently, the use of GNRs for FETs depends on the ability to mitigate the size effect, which follows two general approaches. In one approach, synthesis or patterning techniques should be improved to obtain graphene ribbons with smoother edges. In Figure 4.7, the size effect for the lithographically-patterned GNRs of this study is compared with that for the chemically-synthesized GNRs from [81]. In [81], GNRs are produced from the chemical unzipping of CNTs, and are found to have LER < 1 nm (from TEM characterization). As expected, the smoother, chemically-synthesized GNRs see a later onset of the size effect: the knee of the mobility curve occurs at ~20 nm (instead of ~50 nm for the lithographically-patterned GNRs). The trendline for mobility in the chemically-synthesized GNRs is obtained via Equation (4.1). Herein, the $\mu_{lattice}$ and μ_{SiO2} terms are neglected, μ_{imp} = 1450 cm^2/V-s, and $\mu_{LER} = A \cdot W^B$, where A = 0.08 cm^2/V-s, B = 4.0, and W is given in nm.

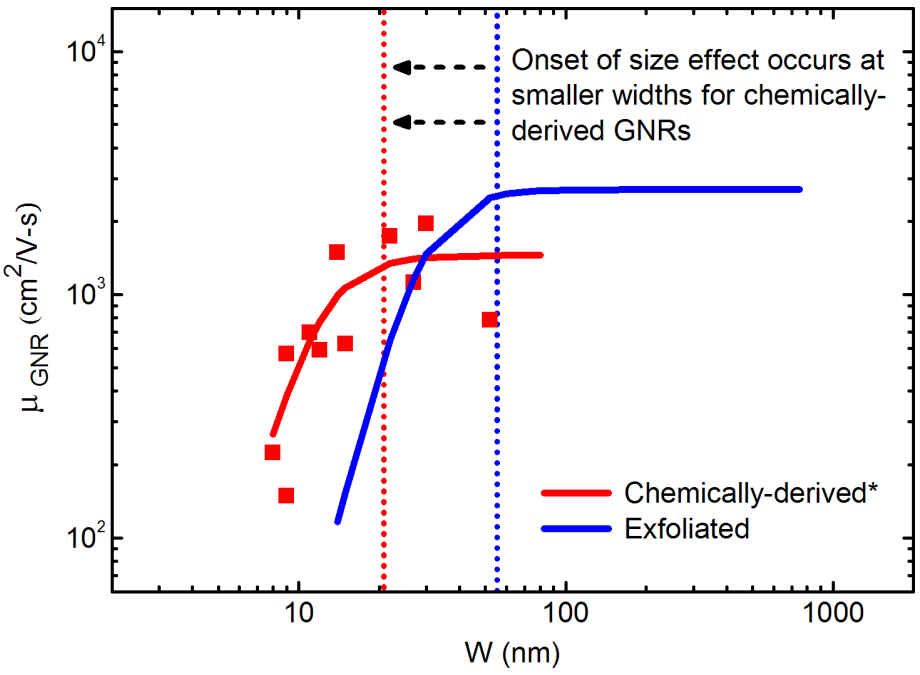

Figure 4.7: Comparison of the size effect in lithographically-patterned and chemically-synthesized GNRs. For chemically-synthesized GNRs with an LER < 1 nm, the onset of the size effect appears at a smaller width compared with the onset for lithographically-defined ribbons with an LER of 2–3 nm in this study. Adapted from [81].

A second approach to mitigate the size effect relies upon passivation techniques that alter the chemical bonds of graphene, converting targeted areas from semimetallic to semiconducting or insulating. The selective passivation of graphene can thus be used to limit the scattering impact of rough edges in GNRs. Chemical modification of graphene, for instance by hydrogenation, has been discussed in terms of bandgap opening [82]. Hydrogenated graphene (graphene) has been experimentally demonstrated on 2D, large-area graphene [83, 84] and 100-nm-wide GNRs [85]. In these studies, carbon atoms on the basal plane of graphene regions are hydrogenated. In the present study, a fabrication process flow is developed to utilize this hydrogenation technique for carbon atoms at the edges of graphene ribbons. This hydrogenation process passivates the dangling bonds of edge atoms and potentially converts targeted areas from metallic to insulating. It is thus

expected that carriers prefer a path through the unaffected center of the graphene ribbon, bypassing scattering centers along the rough edges [86].

Graphene flakes are deposited onto a 300 nm SiO_2 film. EBL and a metal liftoff process define the contacts electrodes and a second EBL step and a plasma etch define the GNRs. Hydrogenation is achieved by exposing graphene to a low-power hydrogen plasma in a RIE tool. To avoid etching of graphene during hydrogenation, a machined shield structure is used to protect the sample. Openings (0.5 in. by 0.2 in.) on each side of the shield are large enough to let ions pass through for hydrogenation but small enough to prevent direct ion milling. This is verified by observing that graphene flakes exposed to the hydrogen plasma for 10 min. without the shield are fully etched while flakes exposed under the same conditions for 1 hr. with the shield remain intact. After hydrogenation (RIE settings: 11 W for 5 min.), the D-peak at 1342 cm^{-1} sharply increases (Figure 4.8), signifying the conversion of sp^2-bonds into sp^3-bonds, while two small peaks at 1620 cm^{-1} (D') and 2950 cm^{-1} (D+D'), also attributed to hydrogenation [83], are witnessed. Hydrogenation is stable for at least 3 days in the ambient environment, as shown by the identical Raman spectra obtained after this period. Reversal of the hydrogenation process is achieved by annealing the devices in an argon environment (300° C; 600 Torr) for 30 min. The D' and D+D' peaks are no longer visible while the D-peak is minimal. No significant changes in the 2D-peak are observed, indicating that graphene has not been inadvertently etched during hydrogenation. The results indicate that bilayer graphene is more susceptible to hydrogenation than single-layer graphene.

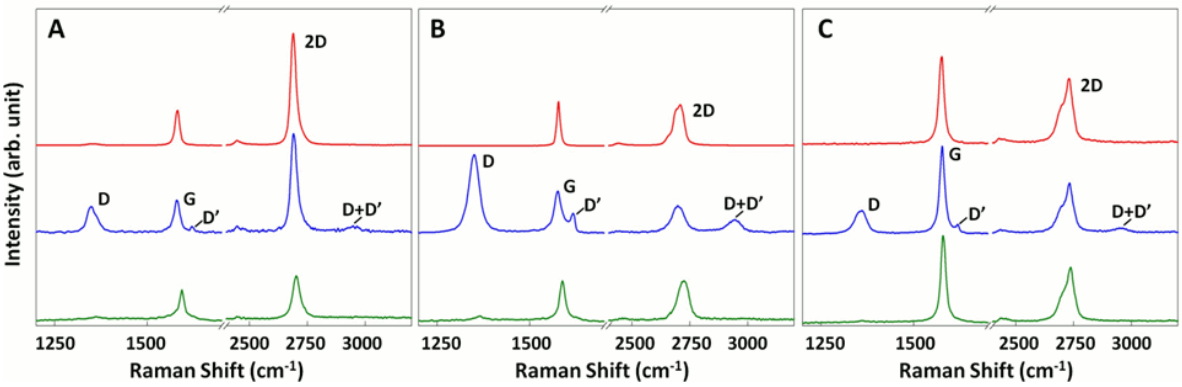

Figure 4.8: Evolution of Raman spectra of hydrogenated graphene for (a) SLG (b) BLG and (c) FLG. The red, blue and green curves (from top to bottom) correspond to pristine, hydrogenated and annealed devices, respectively.

GNRs are covered by a negative-tone e-beam resist, HSQ. To expose the ribbon edges only, devices are exposed to a dilute (0.1%) HF solution for 5 sec. SEM imaging before and after HF exposure confirms the etching of the HSQ ribbon (at a rate of ~1 nm/sec.) along its periphery (Figure 4.9). Finally, the devices are immediately placed into the plasma tool for hydrogenation. Since GNR edges are more chemically reactive than the graphene basal plane, hydrogenation time is reduced to 2 min.

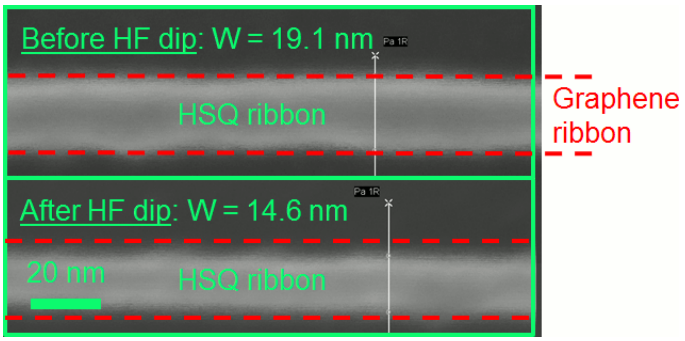

Figure 4.9: SEM image of HSQ "trimming" process (via HF). Before the trim, the width of the HSQ structure is ~19 nm; after trimming (5 sec. bath in 0.1% HF solution), the width is reduced to ~15 nm. The dashed red lines in the image indicate the outline of the GNR, which does not interact with HF.

Back-gated testing is performed for single- and bi-layer GNRs at three stages of the process flow: (i) after etching of the GNR devices, (ii) after trimming of the HSQ ribbons, and (iii) after hydrogenation. In each device, the minimum conductivity point is found to shift to more negative voltages after hydrogenation. In addition, the electron-doping is more severe for BLG. The larger electron-doping for BLG corroborates the hydrogenation results on large-area graphene (that BLG is hydrogenated more readily than SLG). Electrical testing before and after HSQ trimming (but prior to hydrogenation) confirms that the negative shift of $V_{g,min}$ is a result of hydrogenation and not of trimming. In fact, after HSQ trimming, a slight positive shift of $V_{g,min}$ is observed in both devices. Mobility is calculated as $\mu = \sigma/(n \cdot e)$, where n is induced carrier density and σ is device resistivity. Room-temperature mobility is found to improve by up to 50% at an electron density of 5×10^{12} cm^{-2}.

4.6 Conclusion

Nanoscale graphene provides a platform to integrate high-density circuitry with suitable characteristics for digital logic (i.e., a semiconducting bandgap). As graphene is patterned via lithography and plasma etching into a GNR less than 50 nm wide, rough edges result in increased scattering and degraded mobility. The more aggressively these GNRs are scaled, the larger the impact of their edges. In this study, while a mobility of ~3000 cm^2/V-s is readily achieved for ribbons with $W > 50$ nm (limited by impurity scattering), this value decreases to less than 200 cm^2/V-s for ribbons with $W < 20$ nm (limited by edge scattering). This crossover point between impurity-limited mobility and LER-limited mobility depends on the extent of LER and of impurity density. For GNRs

with comparable n_{imp} but lower LER, the size effect would be less pronounced (it sets in at a smaller width). For GNRs with comparable LER but lower n_{imp}, the size effect would be more pronounced (it sets in at a larger width). As this crossover point is observed at technologically-relevant dimensions (for scaling), graphene FET electronics depends on the ability to mitigate the size effect. Mitigation of the size effect assumes one of two approaches: (i) synthesize or pattern GNRs with smoother edges or (ii) passivate rough edges to reduce the impact of these edges on transport. Section 4.5 develops a technique to selectively passivate GNR edges through hydrogenation. HSQ ribbons are trimmed to expose the underlying GNR edges. Then, exposure to a low-power hydrogen plasma modifies the exposed GNR edges, converting sp^2-bonded carbon to sp^3-bonded carbon. As carriers are directed away from these rough edges, this technique can be used to improve carrier mobility in graphene nanoribbons.

CHAPTER 5

VARIATION IN GRAPHENE DEVICES

5.1 Introduction

Graphene's high surface area to volume ratio and excellent mechanical strength [27] make it a compelling material for sensing applications. From a device perspective, such sensitivity demands meticulous handling and processing to minimize unintentional modification of device characteristics. In a graphene VLSI chip, little device variation can be tolerated. To manage this variation, two sources of device-to-device variation are investigated: (i) atmospheric adsorbates, composed of molecular oxygen and water, in exfoliated graphene on SiO_2 and (ii) substrate-induced disorder in epitaxial graphene on SiC. Insight into the electrical behavior of graphene exposed to atmosphere elucidates the doping role played by the atmosphere. In epitaxial graphene, ridge-like terraces imposed by the SiC substrate render the material to be polycrystalline. It is thus essential to study how this disorder affects carrier transport, and the consequences for device design.

5.2 Influence of Atmosphere on Electrical Transport in Graphene

A number of doping and sensing studies in graphene have involved the exposure of dopant species in gaseous form [33, 87, 88] or in solution [89, 90] though none have been dedicated to atmospheric effects. Based on these experiments, the following points are evident. First, graphene transport is governed by short and long-range scattering at high- and low-carrier density, respectively. The crossover between the two regimes is

marked by the transition from a linear I-V (long-range scattering) to a sub-linear I-V (short-range scattering). Second, conductivity approaches $4 \cdot e^2/h$ in devices with large impurity density. For clean devices, this minimum conductivity (σ_{min}) is larger and more sensitive to fluctuations of impurity density. Further, the width of σ_{min} is governed by inhomogeneous charge puddles [42]. Third, doping influences graphene by introducing extra charges as well as scattering sites, thereby increasing the charge density but also causing additional scattering. In [91], ionic screening of substrate impurities in graphene was investigated by exposing graphene to a solution of NaF. Upon exposure, $V_{g,min}$ shifts from +30 V to near 0 V and mobility improves. In [87], increased potassium doping of graphene is seen to degrade mobility by an order of magnitude as $V_{g,min}$ shifts from –9 V to –80 V. The findings of both studies fit neatly into long-range scattering theory [92]: effects of charged substrate impurities are neutralized via ionic screening and this leads to a mobility improvement. Dopants may improve transport by acting as compensators—they reduce scattering by neutralizing existing impurities. Interestingly, all previous work points to a decrease (increase) in mobility with an increase (decrease) in doping. This suggests that it is difficult to employ a dopant to improve mobility (by screening existing impurities) while simultaneously increasing doping density. In this study, the interaction of the atmosphere, composed of O_2 and ambient air, and substrate impurities is shown. The findings illustrate, with increasing atmospheric exposure, that hole-doping increases while mobility can increase or decrease depending on the nature of substrate impurities. The results provide a basis for understanding variation in graphene devices on SiO_2.

Exfoliated graphene is prepared on a 300 nm SiO_2 substrate. After patterning of contact electrodes, the as-prepared flakes are exposed to the atmosphere—composed of

molecular oxygen (99.99% purity) and ambient air with 55% relative humidity (at this humidity level, water accounts for 1% of ambient air by mass). A number of devices were studied and four atmospheric doping cases involving three distinct devices (labeled D1–D3) are presented—these four cover a range of device quality and doping behavior when exposed to the atmosphere, Figure 5.1. Herein, it is desirable to look at the behavior of not just high-quality devices because a comprehensive evaluation of the influence of atmospheric doping is sought. Prior to all experiments, devices are degassed (pressure $\leq 10^{-5}$ Torr) inside the test chamber for 10 hr. to drive out residual adsorbates. Two types of doping experiments are performed with device D1. In the first experiment, termed run-A, the test chamber is opened, leaving the device exposed to the ambient air. In the second experiment, run-B, the device is exposed to both O_2 and ambient air. Initially, the device remains inside the test chamber while O_2 is introduced at a flow rate of 20 sccm. During O_2 exposure, the pump is disconnected so the chamber pressure increases with the inflow of oxygen; the chamber pressure reaches atmospheric pressure after 30 min. Once at atmospheric pressure, the chamber remains closed so the graphene device continues to be exposed to oxygen. After nearly 110 min. of O_2 exposure, the flow is cut off; the test chamber is opened and the device is exposed to ambient air for further testing. Devices D2 and D3 are subject to run-A only (O_2 exposure). Back-gated I-V data are recorded every 2 min. The response of drain conductivity (σ_{ds}) vs. applied gate bias (V_{gs}) for each experiment is described as follows.

Case 1: A moderate-quality device (D1: W / L = 16 μm / 4 μm) is subject to run-A. At the start of ambient exposure, $V_{g,min}$ = +10 V and σ_{min} = 8.5 e^2/h; after 141 min. of ambient exposure, $V_{g,min}$ = +46 V and σ_{min} = 5.5 e^2/h.

Case 2: D1, having undergone vacuum desorption to reverse the effects of run-A, is subject to run-B. After 9 min. of oxygen exposure, $V_{g,min}$ = +10 V and σ_{min} = 7.9 e^2/h; after 110 min. of oxygen exposure $V_{g,min}$ = +26 V and σ_{min} = 6.6 e^2/h. At this point, O_2 flow is discontinued and the device is directly exposed to the ambient. The doping behavior remains qualitatively the same as before (i.e., hole-doping occurs) but the rate of doping increases. The rate of doping during ambient exposure could be higher since moisture is thought to promote hole-doping by O_2 [93] . In total (after 110 min. of O_2 exposure followed by 106 min. of ambient exposure), $V_{g,min}$ and σ_{min} shift to +39 V and 5.4 e^2/h, respectively.

Case 3: A different moderate-quality device (D2: W / L = 5 μm / 2 μm) is subject to run-A. Upon ambient exposure, $V_{g,min}$ increases from +8 V to +31 V while σ_{min} decreases from 6.2 e^2/h to 4.5 e^2/h. Near the end of the exposure, a minor kink in the conductance curve appears.

Case 4: A high-quality device (D3; W / L = 1 μm / 3 μm) is subject to run-A. The device shows the expected hole-doping with increasing ambient exposure. After more than 2 hr. of ambient exposure, $V_{g,min}$ increases from –15 V to +16 V; σ_{min} remains nearly constant.

In addition to oxygen and the ambient, these devices are exposed to nitrogen. After continuous nitrogen flow (for nearly 1 hr.) to the test chamber, little change in the σ_{ds}-V_{gs} plot. This result suggests that O_2 and water are the primary species in the atmosphere responsible for doping graphene, and is consistent with previous observations [94-97].

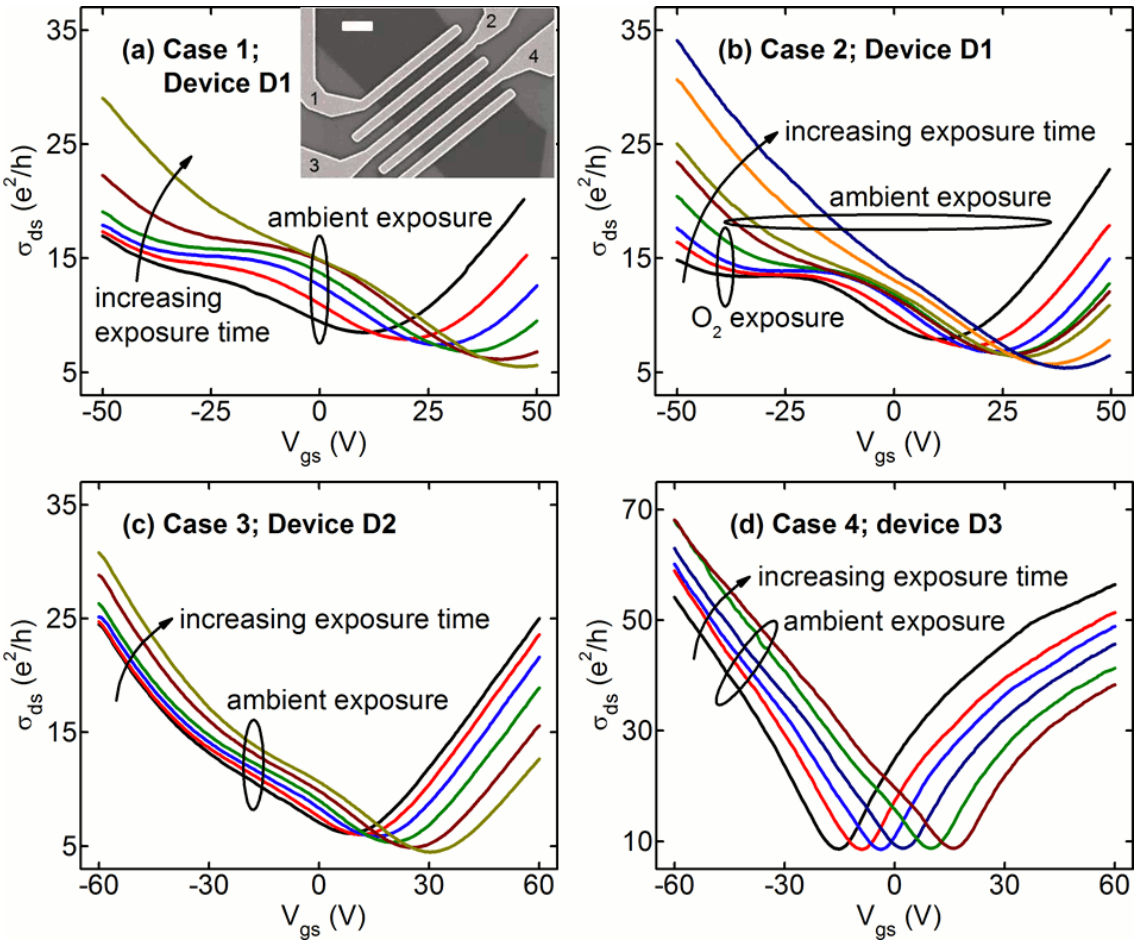

Figure 5.1: σ_{ds}-V_{gs} behavior for four separate doping experiments. In case-1 (a), D1 is subject to run-A, or ambient exposure; σ_{ds}-V_{gs} is plotted for 3, 9, 18, 36, 74, and 141 min. of ambient exposure. In case-2 (b), D1 is subject to run-B. The device is first exposed to O_2 for 112 min.; σ_{ds}-V_{gs} is plotted for 9, 24, 52, and 112 min. of O_2 exposure. It is then exposed to the ambient for another 104 min.; σ_{ds}-V_{gs} is plotted for 1, 12, 64, and 104 min. of ambient exposure. In case-3 (c), D2 is subject to run-A; σ_{ds}-V_{gs} is plotted for 4, 9, 15, 39, 100, and 171 min. of ambient exposure. In case-4 (d), D3 is subject to run-A; σ_{ds}-V_{gs} is plotted for 5, 10, 20, 35, 105, and 135 min. of ambient exposure (d). An SEM image of D1, with electrodes contacting the graphene sheet, is shown in the inset to (a). Four-point testing is conducted across the four electrodes denoted in the image (scale bar = 1 μm).

To understand the influence of these atmospheric adsorbates on transport, it is useful to consider the broader scope of scattering mechanisms in graphene. The scattering mechanisms detailed in Section 2.2 are revisited: (i) lattice phonon scattering that limits mobility to 2×10^5 $cm^2/V\text{-}s$, (ii) remote phonon scattering from the SiO_2 substrate that

limits mobility to 4×10^4 cm^2/V-s, and (iii) impurity scattering at the graphene-substrate interface. Edge scattering is neglected since the devices in this study have widths on the μm-scale. Overall mobility can be written as

$$\frac{1}{\mu} = \frac{1}{\mu_{lattice}} + \frac{1}{\mu_{SiO2}} + \frac{1}{\mu_{imp}} \tag{5.1}$$

With mobilities in the range of 1000–4000 cm^2/V-s and a linear conductance behavior at high carrier density ($n \geq 4\times10^{12}$ cm^{-2}), it is apparent that substrate impurities play a dominant scattering role for devices in this study. The assumption of impurity-limited transport allows conductivity to be expressed as follows [29]:

$$\sigma(n-\overline{n}) = \begin{cases} 20\cdot\frac{e^2}{h}\cdot\frac{n^*}{n_{imp}}, & if\ n-\bar{n} \leq n^* \\ 20\cdot\frac{e^2}{h}\cdot\frac{n}{n_{imp}}, & if\ n-\bar{n} > n^* \end{cases} \tag{5.2}$$

where n is the induced carrier density, n_{imp} is the impurity density, $\bar{n}$ is the carrier density at $V_{gs} = V_{g,min}$, and n^* characterizes the width of the minimum conductivity plateau.

Figure 5.2a plots $V_{g,min}$ vs. exposure time for the experiments of case-2 through case-4. Under atmospheric exposure, $V_{g,min}$ shifts significantly to more positive voltages, indicative of hole-doping—with the steepest shifts seen in the first 30 min. of exposure. After 2 hr. of exposure, the effect of hole-doping of graphene by atmospheric adsorbates begins to saturate. In case-2, the doping behavior shows two trends; there is a noticeable increase in the shift of $V_{g,min}$ when O_2 exposure ends and ambient exposure begins. For all devices, it was possible to bring σ_{ds}-V_{gs} back to nearly its original state (before doping) after prolonged (> 10 hours) vacuum desorption. For example, with D1 subject to run-A, $V_{g,min}$ shifts from +10 V to +46 V. After vacuum desorption, $V_{g,min}$ falls back to +8 V and the σ_{ds}-V_{gs} plot qualitatively matches that from before run-A. That vacuum desorption

carried out at room temperature restores the effects of atmospheric doping suggests that these adsorbates interact with graphene through a physisorption or weak chemisorption process such as dipole-dipole interactions. (It should be noted though that after repeated cycling of ambient exposure followed by vacuum desorption, a small but non-reversible doping effect is seen.) This result is supported by theoretical studies that discuss a weak charge transfer between O_2 and carbon nanotubes [98, 99] or between water and graphene [95, 97, 100].

Next, the influence of atmospheric doping on mobility, extracted via the relation $\mu = \sigma/(n \cdot e)$, is examined. This method of extracting mobility is valid for carrier densities $\geq 4\times10^{12}$ cm^{-2}, for which conductivity approaches a linear-in-density form. Figure 5.2b shows hole mobility (μ_{hole}) vs. exposure time for the experiments of case-2 through case-4, extracted at a hole density of 4×10^{12} cm^{-2}. (Hole mobility is used, rather than electron mobility, since doping causes a significant hole-shift of the σ_{ds}-V_{gs} plot. Thus, within the applied gate bias range, the range of induced electron densities is limited.) For case-2, μ_{hole} increases by 36%—from 845 to 1152 cm^2/V-s—after 216 min. of total atmospheric exposure. This increase suggests that adsorbates compensate for substrate impurities in case-2. Meanwhile, μ_{hole} reduces by 16% after 171 min. of exposure for case-3 and by 21% after 135 min. of exposure for case-4. The reciprocal relation between mobility and n_{imp} is noted by inserting Equation (5.2) into the mobility expression

$$\mu = 20 \cdot \frac{e^2}{h} \frac{1}{n_{imp} \cdot e} \tag{5.3}$$

The calculated range of n_{imp} is from $1.2–1.6\times10^{12}$ cm^{-2} for the high-quality device (D3) and from $4.2–5.7\times10^{12}$ cm^{-2} for the moderate-quality devices (D1 and D2).

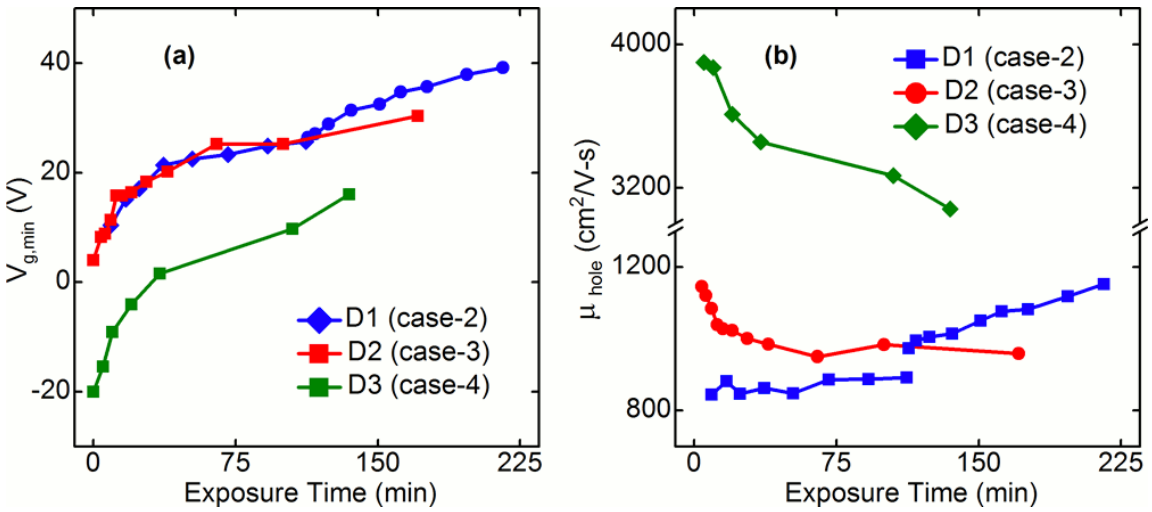

Figure 5.2: Shift in $V_{g,min}$ and μ_{hole} upon atmospheric doping. $V_{g,min}$ vs. exposure time (a) and μ_{hole} vs. exposure time (b) are plotted for cases 2–4. Rapid hole-doping occurs under both O_2 and ambient exposure. The trendline for case-2 is broken into two to distinguish between the effect of doping with O_2 flow (first half of exposure) and doping with ambient air (second half of exposure). Hole mobility is seen to increase for device D1 under both O_2 and ambient exposure.

In D2 (case-3) and D3 (case-4), ambient exposure results in a decrease in hole mobility. On the other hand, D1 (case-2) shows an increase in μ_{hole} with O_2 and ambient exposure; this case also features a prominent kink in the σ_{ds}-V_{gs} plot that disappears with increased hole-doping. Interestingly, for case-2, adsorbates play a dual role of hole-dopant (expressed by a positive shift of $V_{g,min}$) and charge screening layer (expressed by an increase in mobility). To illuminate the device-to-device variation and the changing behavior of each device under atmospheric exposure, a phenomenological but physically-intuitive model is developed. In exfoliated graphene on SiO_2, it is well-known that substrate impurities lead to electron-hole puddles in graphene [42]. This situation fairly accurately describes the devices in this study since mobility is impurity-limited. In this model, graphene sheets are divided into a collection of p- and n-regions corresponding to the type of substrate impurity dominating in that region. Several assumptions need to be

made even in a basic model such as this. First, what parameters should be used for the p- and n-regions? To simplify the model, all p-regions are assumed to be homogeneous, as are all n-regions, though the two regions are distinct from one another. Second, should percolation theory or a resistor network [101] be used to model transport properties? The latter is used since it has been shown that percolation theory is not needed to model the system of impurities affecting graphene conductance [102]; p-n junctions are modeled to be ballistic. Third, using a resistor network model, how many regions should be assumed to be p-type, how many to be n-type, and how should they be configured (e.g., in series or in parallel)? Simple case studies are used to identify which gives the best fit to the data. Conductivity of each distinct p- and n-region, from Equation (5.2), is modeled as

$$\sigma(V_{BG}) = \begin{cases} \sigma_{min}, & if\ V_{BG} - V_{g,min} \leq V^* \\ \sigma_{min} + s \cdot \left(\left| V_{BG} - V_{g,min} \right| - V^* \right), & if\ V_{BG} - V_{g,min} > V^* \end{cases} \quad (5.4)$$

where V^* characterizes the width of the minimum conductivity plateau, an indication of device quality. In each region, the adjustable parameters $V_{g,min}$, σ_{min} and s are found semi-empirically. For instance, the position of the kink and minimum conductivity point of case-2 guides the selection of $V_{g,min}$ and σ_{min} for the p- and n-regions of the model. The parameter s is used as a fitting parameter to find the best fit between model and experiment. By comparing Equations (5.2) and (5.4), it is seen that s in Equation (5.4) plays the role of $1/n_{imp}$ in Equation (5.2). That is, s reveals information about device quality (a higher s indicates a higher-quality device). Finally, V^* is analogous to n^* from Equation (5.2), and thus related to n_{imp} [29]. A higher-quality device exhibits a sharper minimum conductivity point (with a smaller plateau). Thus for the moderate-quality devices (D1 and D2), V^* is set to 6 V while for the high-quality device (D3), V^* is set to

3 V. All model parameters used to fit the atmospheric doping experiments are listed in Appendix B.

The resistor network model is used to illustrate the electrical response of these devices to atmospheric exposure; the model fitting is performed at the beginning and end of the exposure. Figure 5.3a-b compares σ_{ds}-V_{gs} as generated by the model to that from experiment for case-2 and case-4. For D1 in case-2 (Figure 5.3a), it is seen that a series connection of p-, n-, and p-regions leads to a robust model that brings out the key features of the σ_{ds}-V_{gs} plot. The model is able to portray the kink behavior observed at the start of O_2 exposure and the disappearance of the kink at the end of ambient exposure. For D3 in case-4 (Figure 5.3b), an optimal configuration is found using a series connection of n-, p-, and n-regions. In Figure 5.3c, n_{imp} vs. exposure time is plotted for the distinct p- and n-regions of the model in case-2 and case-4; n_{imp} changes with doping as a result of charge transfer from the adsorbates to the graphene. Here, n_{imp} can be viewed as an effective impurity density that characterizes the combined doping from the adsorbates and the substrate impurities, as well as the interaction of adsorbates and impurities. Comparing n_{imp} before and after doping for case-2, n_{imp} of the p-region decreases from 3.6×10^{12} to 3.2×10^{12} cm^{-2} while n_{imp} of the n-region increases from 3.2×10^{12} to 3.4×10^{12} cm^{-2}. For case-4; n_{imp} of the p-region also decreases, from 2.8×10^{12} to 1.8×10^{12} cm^{-2}, and n_{imp} of the n-region also increases, from 0.8×10^{12} to 1.6×10^{12} cm^{-2}.

That p-regions (n-regions) observe a decrease (increase) in n_{imp} with increased atmospheric doping suggests that adsorbates mitigate (heighten) carrier scattering in the p-regions (n-regions). This behavior is understood in terms of the interaction between atmospheric adsorbates and substrate impurities, Figure 5.3d. In particular, there is an

interaction asymmetry in the following cases: (i) repulsion between negatively-charged adsorbates (since these adsorbates donate holes to graphene) and negatively-charged substrate impurities (underneath p-regions of graphene) and (ii) attraction between negatively-charged adsorbates and positively-charged substrate impurities (underneath n-regions of graphene). In the first case (in p-regions of graphene), two like charges are on opposite sides of the graphene sheet; their electric field components transverse to the basal plane cancel and mobility increases. In the second case (in n-regions of graphene), positive and negative charges are on opposite sides of the graphene sheet—carriers thus experience a larger potential and mobility decreases. Consequently, devices consisting mainly of p-regions would see overall mobility improve while devices consisting mainly of n-regions would see overall mobility decrease.

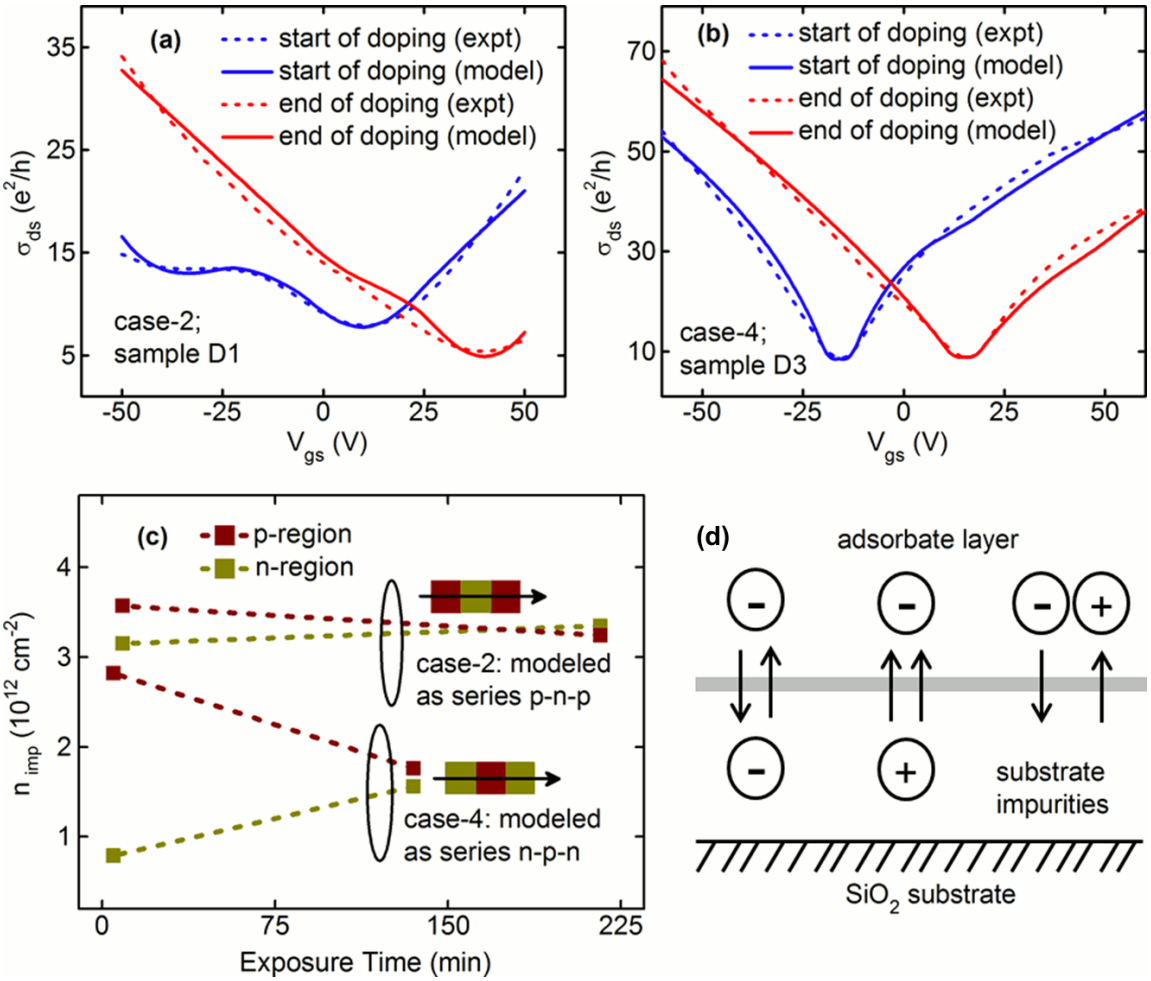

Figure 5.3: A model for the response of graphene to atmospheric doping. A resistor network of p- and n-regions is used to model the electrical response of graphene to atmospheric exposure. For D1 in case-2 (a), a series connection of p-, n-, and p-regions is used to model the key features of σ_{ds}-V_{gs}. For D3 in case-4 (b), an optimal configuration is found using a series connection of n-, p-, and n-regions. In each case, the model for σ_{ds}-V_{gs} is shown at the start and end of the doping experiment; the results compare well to experiment. In (c), n_{imp} vs. exposure time is plotted for the p- and n-regions represented by the models for case-2 and case-4. With increasing atmospheric exposure, it is seen that the p-regions show a decrease in n_{imp} while the n-regions show an increase in n_{imp}. In (d), a physical model of the interplay between adsorbates and substrate impurities is used to understand the transport properties of these doping studies.

5.3 Binding Mechanisms of Molecular Oxygen and Moisture to Graphene

Although the last section addressed the doping behavior of graphene exposed to atmospheric adsorbates, there remains a lack of understanding in how this doping occurs.

Leenaerts *et al.* [103] predicted that, for water, there is a fractional charge transfer of 0.025 electrons per molecule from graphene to the adsorbate (thus, hole-doping occurs). Lu *et al.* [104] estimated that molecular oxygen hole-dopes free-standing graphene with a fractional charge transfer of ~0.1 electrons per molecule (from graphene to the adsorbate). Another study [105] showed that molecular oxygen bonded to SiO_2 has an electrostatic interaction energy on the order of 100 meV. This strong interaction, in turn, leads to a higher fractional charge transfer to graphene. In [93], hole-doping of graphene is attributed to O_2 trapped at the graphene-SiO_2 interface. This doping by O_2 is enhanced by water (i.e., water acts as a catalyst for oxygen doping). This study elucidates the binding mechanisms of oxygen and moisture to graphene.

The experimental setup in this study is similar to that for Section 5.2 (exfoliated graphene on a 300 nm SiO_2 substrate). Back-gated electrical testing is carried out for devices under exposure to: (i) molecular oxygen (99.99% purity) and (ii) the ambient (55% relative humidity). Graphene is exposed to oxygen by a controlled flow into the chamber; once O_2 inflow brings the chamber to atmospheric pressure, the chamber is opened to the ambient. Overall, five more devices are studied and each falls into one of two batches. The first batch showcases thin graphene, single- or bi-layer graphene, while the second features few-layer graphene (8 layers thick). Tracking of $V_{g,min}$ reveals that SLG and BLG undergo hole-doping under both O_2 and ambient exposure while FLG undergoes hole-doping primarily under ambient exposure. In the SLG device, $V_{g,min}$ shifts rapidly (compared to the BLG and FLG devices) under O_2 exposure, Figure 5.4; hole-doping continues upon ambient exposure. For BLG, $V_{g,min}$ shifts at a more moderate pace under O_2 exposure; hole-doping continues upon ambient exposure. Meanwhile, both FLG

devices reveal a small $V_{g,min}$ shift (< 1 V) under O_2 exposure. The shift in $V_{g,min}$ indicates a net hole transfer of 4×10^{11} cm^{-2}, 2×10^{11} cm^{-2}, 0.5×10^{11} cm^{-2} after 50 min. of O_2 exposure for single-, bi-, and few-layer graphene, respectively. Under ambient exposure, meanwhile, a net hole transfer of $1.5–3\times10^{10}$ cm^{-2} for every min. is observed, for all graphene thicknesses. By observing the different rates of hole-doping under these two environments, it is posited that doping under O_2 exposure occurs on the basal plane of graphene while doping under ambient exposure occurs predominantly at the edges of the graphene flake. Since the FLG devices are 8 layers thick, a nearly order of magnitude higher doping rate in SLG compared to that in FLG is expected if doping by O_2 indeed occurs at the surface of the flake.

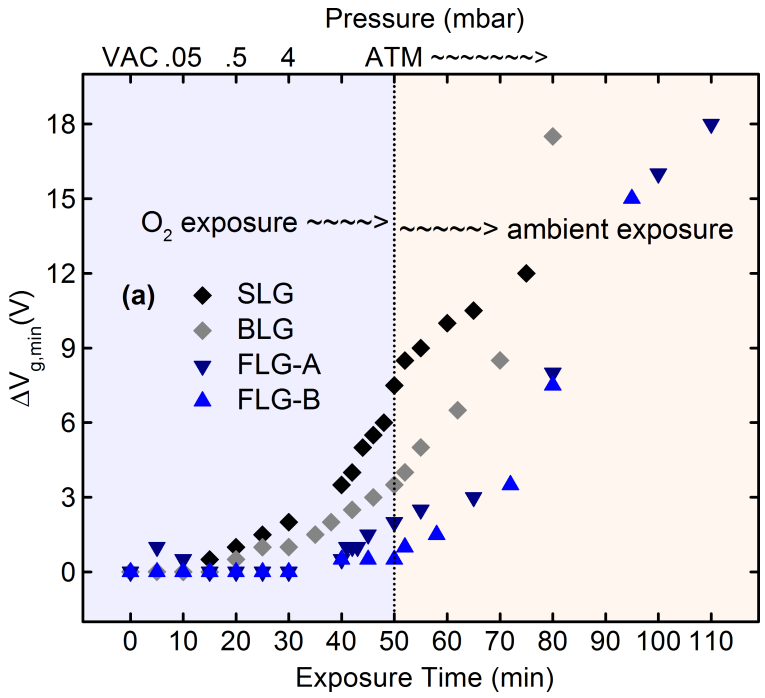

Figure 5.4: Response of thin and thick graphene to O_2 and ambient exposure. Both environments induce hole-doping in graphene. Under O_2 exposure, a thickness-dependent hole-doping rate is seen—SLG is doped rapidly, BLG moderately, and FLG (8 layers thick) minimally. On the other hand, under ambient exposure, the hole-doping rate is similar in graphene devices of varying thicknesses.

Mobility—extracted at a carrier density of 3×10^{12} cm^{-2}—is found in the range of 2200–8500 cm^2/V-s for these devices. Figure 5.5 plots mobility for a SLG device and a FLG device upon O_2 and ambient exposure. For both devices, mobility remains invariant under O_2 exposure. For SLG in ambient, electron and hole mobility sharply increase and continue to rise upon further ambient exposure. In the FLG devices studied in this work, no general trend can be identified as mobilities fluctuates upon exposure to the ambient. A minimal shift in $V_{g,min}$ and σ_{min} of FLG upon exposure to O_2 for up to 1 hr. indicates that exposure to the ambient leads to stronger hole-doping of graphene than exposure to O_2. It is predicted that water molecules do not directly dope graphene but act as a catalyst for oxygen doping [93]. The results indicate that moisture in the ambient interacts with the edge atoms of the graphene flake and, in doing so, hole-dopes the graphene.

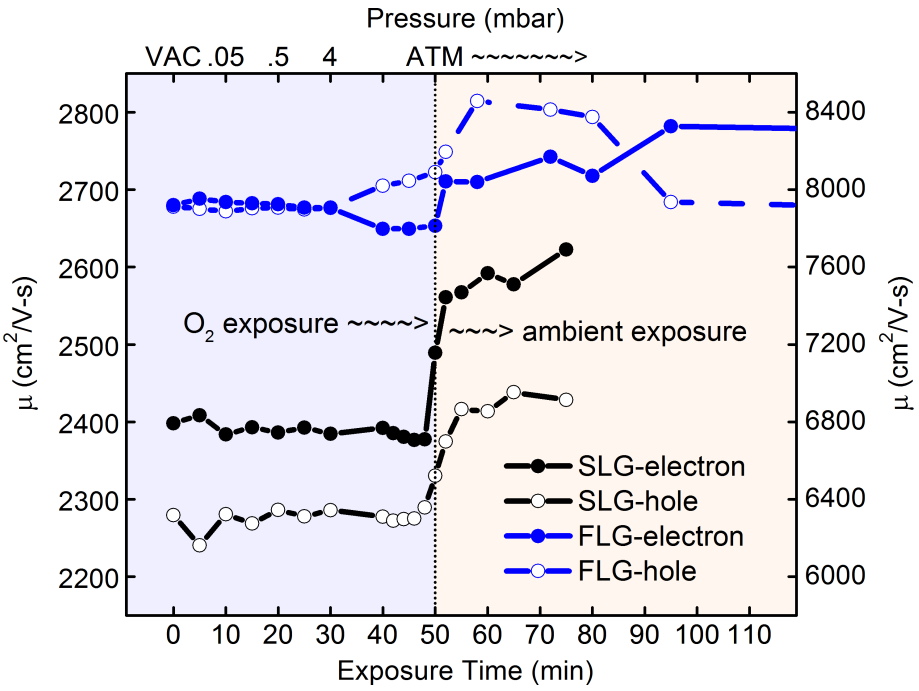

Figure 5.5: Shift in mobility with doping for a SLG device and a FLG device. For both devices, the mobility remains invariant under O_2 exposure. After SLG is introduced to the ambient, both electron and hole mobility sharply increase and then continue to rise upon further ambient exposure.

5.4 Morphology-Dependent Transport in Epitaxial Graphene

The tremendous improvement of the epitaxial graphene platform [106] has given the semiconductor industry a viable manufacturing solution to move graphene beyond a laboratory curiosity. However, from a device perspective, the poly-crystalline nature of epitaxial graphene presents its own challenges. These grains result from the underlying substrate morphology and the graphitization process, and present an additional scattering source not seen for exfoliated graphene. Previous studies [107, 108] revealed anisotropic transport behavior in epitaxial graphene due to scattering off ridge-like terraces imposed by the SiC substrate. In [108], anisotropy is attributed to silicon defects at the terrace boundaries. In the present study, the poly-crystalline nature of epitaxial graphene grown on the Si-face of SiC is analyzed in terms of the graphene film's thickness and doping characteristics, and the implications for device design and fabrication.

To study morphology-dependent transport, epitaxial graphene is grown in an RF induction furnace on 4H-SiC(0001) under vacuum (~10^{-5} Torr) at a temperature of 1600 °C for 10 min. Prior to growth, the SiC substrate is etched in a hydrogen environment at 1400 °C for 30 min. to clean the surface. Raman analysis and van der Pauw testing on as-grown graphene confirm its high quality. Meanwhile, a miscut angle from the polishing of the SiC substrate leads to the formation of ridge-like, terrace step patterns across the surface [109]. Comparison of AFM scans before and after graphitization reveals that the underlying substrate morphology is found to be imparted onto the graphene film. Figure 5.6a shows an AFM image of as-grown graphene with terraces. These terraces have a width in the range of 1–6 μm and generally run parallel to each other across the entire sample (the total sample area is 3.5×3.5 mm^2). The poly-crystalline nature of epitaxial

graphene can be described in terms of these terraces, which represent graphene grains. Based on Raman and AFM analysis, the as-grown graphene also exhibits non-uniform thickness over the terrace steps. Graphene within a terrace is mainly SLG while graphene in proximity to a terrace step is mainly BLG, consistent with previous observations that "bunching" of the graphene film occurs near the terrace steps during growth [110]. Given that strong n-doping is induced by the SiC substrate and the interface layer between the graphene film and the substrate [111], this thickness variation leads to doping variation. For instance in [112], it is seen for FLG (grown on the C-terminated face of SiC) that the bottommost layer is most heavily electron-doped while successive layers (moving away from the substrate) become less and less electron-doped.

To determine the effect of thickness and doping non-uniformity on transport, the transport differences between devices patterned parallel and perpendicular to the terrace steps are studied. GNRs are patterned parallel to (type I) or perpendicular to (type II) terrace steps. A top-gated device with a set of ten parallel ribbons (each with a width of 25 nm and length of 4 μm) is shown in Figure 5.6b. The gate dielectric comprises 30 nm of spin-coated HSQ (the resist is not removed after the graphene etch step) and 100 nm of e-beam evaporated SiO_2. The region of the channel that is directly overlapped by the top-gate is 3 μm long. For this device, an AFM scan after ribbon formation but before top-gate deposition shows that the graphene ribbon straddles a terrace step, Figure 5.6c (it is a type II device). A corresponding cross-section in Figure 5.6d shows that the terrace step is about 5 nm tall. Across all samples, the range of terrace step heights is 3–5 nm. Based on the range of terrace widths (1–6 μm) and step heights (3–5 nm), the miscut angle of the SiC substrate (and thus of the graphene film) is in the range 0.03–0.29 °.

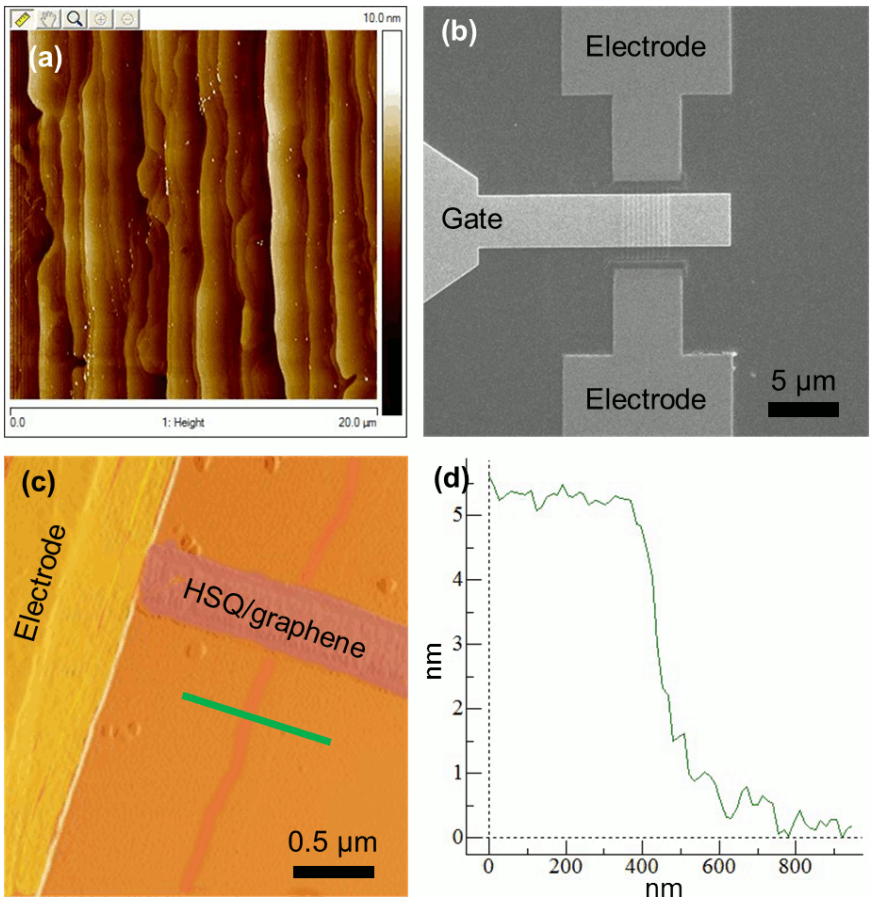

Figure 5.6: Device characterization at various steps of fabrication process: (a) 20×20 μm^2 AFM scan of terrace steps formed in graphene film (after graphitization step), (b) SEM of final device after top-gate formation, and (c) 2.5×2.5 μm^2 AFM scan of a terrace step (visually enhanced by the orange line) that runs underneath the HSQ/graphene ribbon. A cross-sectional profile of the terrace step (green line in (c)) is shown in (d). In this device, the range of terrace widths is 1-3 µm while the step height is around 5 nm. The graphene film is found to be continuous over these terrace steps.

Top-gated I-V measurements are carried out at T = 77 K in high vacuum (~10^{-5} Torr). Representative I-V data are shown for both a type I device and a type II device (Figure 5.7). The device aligned parallel to the terrace step edges (type I device) exhibit the commonly observed I-V behavior with a single minimum conductivity point (or single resistivity maximum). On the other hand, the device aligned perpendicular to the terrace step edges (type II device) exhibit I-V behavior with multiple conductivity

minima (or multiple resistivity maxima). Since the device length (4 μm) is greater than the width of the terraces (1-3 μm) for this type II device, the device is assured to span multiple terraces. Multiple resistivity peaks indicate transport through p-n junctions (that is, polycrystalline graphene can be described in terms of p-n junctions). The presence of distinct junctions is attributed to different doping levels in SLG (heavily electron-doped) and BLG (lightly electron-doped) that form type II devices. It is also found that type II devices exhibit a higher average resistivity (as well as a higher variation in resistivity) compared with type I devices. Taken together, these results indicate that terraces increase scattering (at grain boundaries) and device-to-device variation (as this depends on the number of terraces that the device spans). It is thus critical to account for this anisotropic transport behavior in the design and fabrication of epitaxial graphene devices.

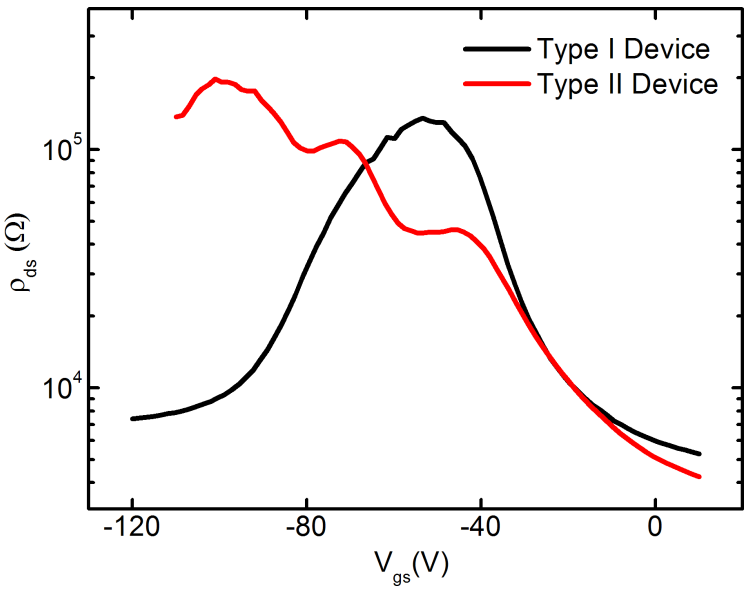

Figure 5.7: Electrical behavior of a type I device (a device aligned parallel to the terrace step edges) and type II device (a device aligned perpendicular to the terrace step edges). ρ_{ds}-V_{gs} data for the type II device show multiple conductance minima, evidence for the role of p-n junctions in electronic transport. In each case, the total device width is 250 nm and length is 4 μm. I-V testing is conducted at T = 77 K in vacuum (~10^{-5} Torr).

5.5 Conclusion

An understanding of the interplay between graphene, its supporting substrate, and atmospheric adsorbates strengthens the design and fabrication of graphene devices. The electrical response of exfoliated graphene exposed to atmospheric adsorbates (oxygen and water) shows that, with increased hole-doping from exposure, mobility can either improve or degrade depending on the nature of substrate impurities. Based on a resistor network model [101], atmospheric adsorbates are predicted to interact with both positive and negative substrate impurities but only compensate for negatively-charged impurities. Next, the binding mechanisms of oxygen and water are studied by observing their doping behavior vs. graphene thickness. Upon O_2 exposure, hole-doping occurs at 0.8, 0.4, and 0.1×10^{10} cm^{-2} per min. for SLG, BLG, and FLG, respectively. Upon ambient exposure, hole-doping occurs at $1.5–3\times10^{10}$ cm^{-2} per min. for all devices. Since doping rates under O_2 (ambient) exposure are inversely proportional to (independent of) graphene thickness, it is suggested that O_2 (ambient) doping occurs on the basal plane (at the edges) of the graphene sheet. The doping effects of O_2 are fully reversible upon anneal and vacuum desorption while the doping effects of the ambient become irreversible with increased exposure time. Finally, in epitaxial graphene, the effect of ridge-like terrace steps on transport is investigated. Due to non-uniform graphene thickness at the terrace step edges, epitaxial graphene exhibits a multi-modal carrier distribution. This is expressed in the electrical behavior of devices that are positioned to straddle terrace steps; these devices exhibit I-V behavior with multiple conductivity minima.

CHAPTER 6

IDENTIFICATION AND ANALYSIS OF A NEW DEVICE PLATFORM: GRAPHENE P-N JUNCTIONS

6.1 Introduction

In the preceding chapters the transport properties of graphene as it evolves from 2D, large-area form to 1D, GNR form were investigated. It appears that opportunities to pursue graphene-based FET electronics are limited. First, GNRs just a few nanometers wide are required for a sizable bandgap. Second, even well above these dimensions the size effect degrades mobility. This chapter approaches graphene electronics not through a drag and drop approach of replacing silicon with graphene but through the development of a device concept based on the unique physics of graphene. In other words, graphene electronics entails the rethinking of material, device, and architectural solutions into an altogether new device platform. This beyond-FET device concept is based on graphene p-n junctions, which manipulate electrons in analogous fashion to how different materials (with different refractive indices) manipulate photons. In particular, these p-n junctions give rise to a tunneling effect for relativistic carriers, the so-called Klein effect, whose tunneling probability depends on the carriers' angle of incidence.

In consideration of a new device concept, the unique physics, device- and system-level performance, and fabrication challenges all have to be addressed together. First, the theoretical underpinnings for the Klein tunneling effect are discussed. Next, the device-level performance of a graphene Klein tunneling device is analyzed using the material's

ideal properties. Based on the results, the system-level benefits of graphene/Klein-based chips is benchmarked against silicon/CMOS-based chips. The experimental feasibility of the Klein device is then addressed through chemical doping.

6.2 Tunneling in Graphene p-n Junctions

The Klein effect, which describes quantum mechanical tunneling for relativistic particles, predicts that carriers striking an energy barrier (with normal incidence) achieve full transmission through the barrier in single-layer graphene but full reflection in bi-layer graphene. The Dirac behavior in graphene is attributed to its lattice symmetry [113]. In particular, the perfect symmetry between the two sub-lattices A and B of graphene's hexagonal lattice produces a "pseudospin" degree of freedom and the conical energy dispersion. This pseudospin index, analogous to the spin index for elementary particles, describes the two-component wavefunctions for carriers in graphene. Thus electron and hole states in graphene are interconnected, and exhibit charge-conjugation symmetry [114]. This is in contrast to carriers in conventional semiconductors, where electrons and holes are described by separate Schrodinger equations.

Charge-conjugation symmetry in graphene allows electrons to manifest as holes and vice-versa. What does this signify for transport in graphene p-n junctions? In single-layer graphene, a right-propagating electron of energy E (and wavevector k) outside a high energy barrier scatters to a left- propagating hole of energy $-E$ (and wavevector $-k$) because of graphene's linear bandstructure [51]. This preserves carrier transport through the energy barrier (a Klein barrier). Bi-layer graphene, by contrast, features a quadratic bandstructure. Matching of an electron and hole is the same situation as described above

enforces that an electron with wavevector k scatters to a hole with wavevector $i \cdot k$ (i.e., an evanescent wave), cutting off carrier transport. These two cases are illustrated in Figure 6.1. Although the tunneling probability through the energy barrier is influenced by the height and width of the barrier, it depends more appreciably on the carriers' angle of approach. Carriers that strike the barrier away from normal incidence witness the collapse of the Klein effect: perfect transmission (reflection) no longer holds for SLG (BLG). For certain angles of approach away from the normal (depending on the doping level of the respective p- and n-regions), carriers fully reflect off energy barriers in SLG and fully transmit across barriers in BLG. This rich tunneling behavior for carriers in graphene can be used to construct a device platform that circumvents the issue of a lack of bandgap, merging the material's high mobility with an excellent on/off current ratio.

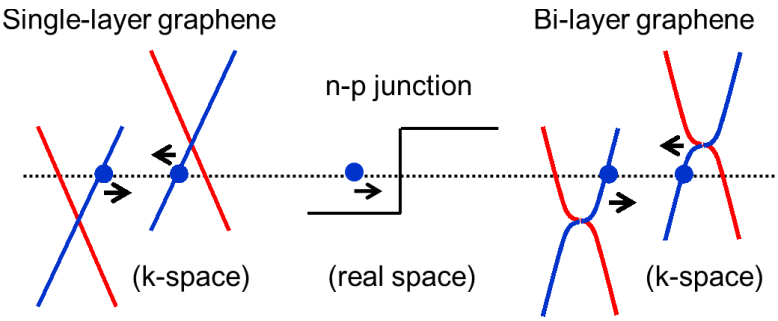

Figure 6.1: The physics underpinning the Klein tunneling effect in graphene. Symmetry of the A and B sublattices in graphene gives rise to a "pseudospin" degree of freedom, manifested as two distinct branches in the bandstructure. The red branch corresponds to one sublattice while the blue branch corresponds to the other. This property is responsible for the peculiar tunneling behavior in graphene p-n junctions.

6.3 Device- and System-Level Evaluation of Graphene p-n Junction Device

As discussed in the previous section, a remarkable feature of graphene is the light-like behavior of its carriers. Using p-n junctions as "waveguides", carriers in graphene can be skillfully controlled and maneuvered. By varying the angle of approach of carriers

with respect to an energy barrier in graphene, the p-n junction acts either as a collimator (transmits carriers) or Klein barrier (reflects carriers). In single-layer graphene, an energy barrier aligned perpendicular to the length of the device acts as a collimator, and the device is turned *on*. On the contrary, an energy barrier aligned diagonal to the length of the device acts as a Klein barrier, and the device is turned *off*. In bi-layer graphene, the opposite tunneling trends are witnessed: an energy barrier aligned perpendicular to the length of the device acts as a Klein barrier while an energy barrier aligned diagonal to the length of the device acts as a collimator. Electrostatic or chemical doping is used to define the doping levels of the p- and n-regions. A gate is then used to actuate the energy barrier, providing the switching mechanism for a graphene Klein tunneling device.

In the device-level analysis of the graphene Klein tunneling device, BLG is the selected platform. An energy barrier aligned perpendicular to the direction of transport acts as a collimator in SLG and a Klein barrier in BLG. Thus bilayer graphene—with a greater capacity to scale junctions—is preferred over single-layer graphene. (A diagonal barrier, for SLG, would unavoidably increase the device length for the same width; see Figure 6.2.) The schematic and associated bandstructure diagrams of the proposed BLG Klein tunneling device are shown in Figure 6.3. In such a device, a top-gate is used to raise and lower the height of the energy barrier, V (in eV), in the channel. In the *on* state, V is below the energy of the incident carriers, E (in eV); as a result, carriers drift from source to drain through an n-n-n junction. In the *off* state, an n-p-n junction forms: V is raised above E, which triggers the Klein effect and cuts off transport in BLG. A key device parameter is θ (Figure 6.3), the angle of approach of the carriers with respect to the normal of the energy barrier.

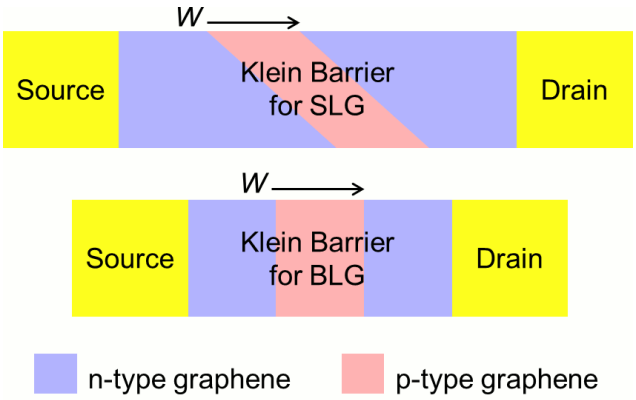

Figure 6.2: Layout of a Klein barrier for single- and bi-layer graphene. SLG has a larger footprint because a diagonally-aligned energy barrier is required to cut off transport.

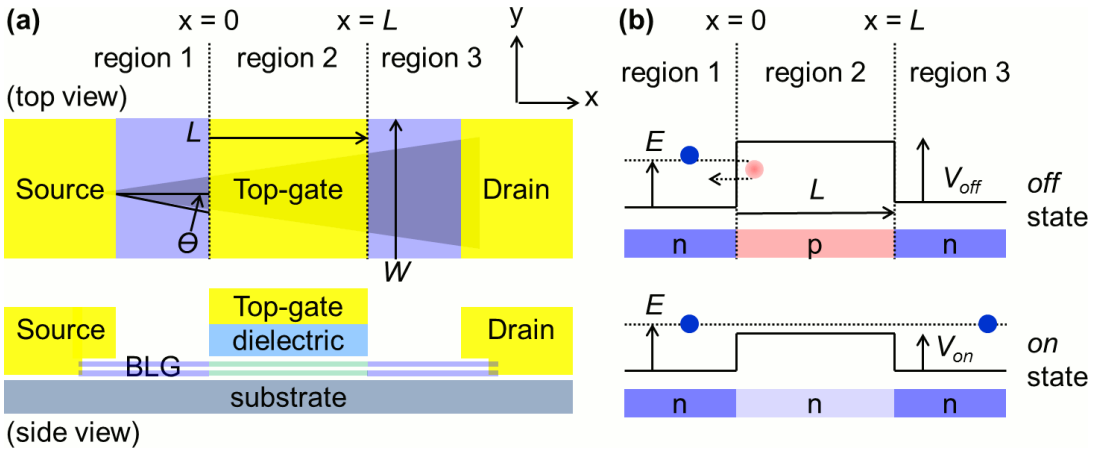

Figure 6.3: Operation of a graphene Klein tunneling device in BLG. For $V > E$, carriers outside the barrier transform into evanescent waves inside the barrier; thus carriers are reflected and the device is in its *off* state. For $V < E$, the Klein effect is not manifested and carriers readily pass through the channel; the device is in its *on* state. The colored tiles represent the doping polarity of graphene: blue for n-doping and red for p-doping.

Tunneling (T) across the energy barrier depends primarily on the carrier's angle of approach, θ (with respect to the barrier's normal), and to a lesser degree on the barrier's height and width. The tunneling of carriers across the barrier in Figure 6.3 is calculated. To begin with, carriers in bi-layer graphene are described by the Dirac-like Hamiltonian [114]

$$H = -\frac{h^2}{8 \cdot m \cdot \pi^2} \cdot \begin{pmatrix} 0 & (k_x - ik_x)^2 \\ (k_x + ik_x)^2 & 0 \end{pmatrix} \tag{6.1}$$

whose eigenstates are expressed as

$$\begin{aligned}\psi_A &= (a_i e^{ik_{ix}x} + b_i e^{-ik_{ix}x} + c_i e^{\kappa_{ix}x} + d_i e^{-\kappa_{ix}x}) \cdot e^{ik_{iy}x} \\ \psi_B &= s_i \cdot \left(a_i e^{ik_{ix}x+2i\phi_i} + b_i e^{-(ik_{ix}x+2i\phi_i)} + c_i h_i e^{\kappa_{ix}x} + \frac{d_i}{h_i} e^{-\kappa_{ix}x}\right) \cdot e^{ik_{iy}x}\end{aligned} \tag{6.2}$$

where s_i = sgn($V_i - E$) and index i represents the region of interest: region 1 for $x < 0$, region 2 for $0 < x < L$ (region of the energy barrier), and region 3 for $x > L$. In general, each eigenstate gives four solutions, two corresponding to propagating waves and two to evanescent waves. Normalization to a_1, amplitude of the right-traveling wave in region 1, and matching of boundary conditions (at $x = 0$ and $x < L$) for each eigenstate and its derivative yields 8 equations with 8 unknowns

$$\begin{aligned} \psi_A^1(x=0) &= \psi_A^2(x=0) & \psi_A^2(x=L) &= \psi_A^3(x=L) \\ \frac{d}{dx}\psi_A^1(x=0) &= \frac{d}{dx}\psi_A^2(x=0) & \frac{d}{dx}\psi_A^2(x=L) &= \frac{d}{dx}\psi_A^3(x=L) \\ \psi_B^1(x=0) &= \psi_B^2(x=0) & \psi_B^2(x=L) &= \psi_B^3(x=L) \\ \frac{d}{dx}\psi_B^1(x=0) &= \frac{d}{dx}\psi_B^2(x=0) & \frac{d}{dx}\psi_B^2(x=L) &= \frac{d}{dx}\psi_B^3(x=L) \end{aligned} \tag{6.3}$$

T is subsequently given by $|a_3|^2$, where a_3 is the amplitude of the propagating wave in region 3. V and E are influenced by background doping, which shifts the Fermi level in their respective regions. Also, V is controlled by electrostatic doping. If $V < E$, Klein effect is not expressed and transport in this case depends on the physics of conventional over-the-barrier scattering.

To verify the operation of the Klein tunneling device for cascading logic, the top-gate must electrostatically dope graphene between $V > E$ (*off* state of device) and $V < E$ (*on* state of device). To determine the energy shift of the potential barrier in BLG induced by electrostatic gating, the following relation is used [18]

$$E_F(n) = \frac{h^2 \cdot n}{2 \cdot m \cdot \pi \cdot g_s \cdot g_v} \tag{6.4}$$

where $m = 0.033 \cdot m_e$ is effective mass of low-energy carriers in BLG [115] (and m_e is electron mass in vacuum), $g_s = g_v = 2$ (spin and valley degeneracy), and n is induced carrier density from Equation (2.1). Using a 2 nm SiO_2 gate dielectric, a gate voltage of 0.5 V shifts E_F by 204 meV. For regions 1 and 3, a background electron doping of n = 3×10^{12} cm^{-2} is chosen, giving E = 108 meV. Next, for region 2, a hole doping of p = 2.8×10^{12} cm^{-2} is chosen, giving V_{off} = 108 meV + 101 meV = 209 meV. (The doping levels prescribed are within range of typical experimental values). To turn the device to the *on* state, V_{gs} is set to 0.5 V: $V_{on} = V_{off} - 204$ meV = 5 meV, ensuring $V < E$. Using these parameters, T is calculated for the device *off* state, Figure 6.4. Markedly, T has a strong angular dependence. Current modulation between *on* and *off* states, I_{on}/I_{off} is $1/T$. A maximum θ (θ_{max}) is defined such that $T(\theta_{max}) < 10^{-5}$, thus ensuring that $I_{on}/I_{off} > 10^5$. This gives $\theta_{max} = 1.89^\circ$ or a total acceptance cone of incident carriers of $2 \cdot \theta_{max} = 3.78^\circ$ (refer to Figure 6.3). See Appendix C for the Matlab code used to generate Figure 6.4.

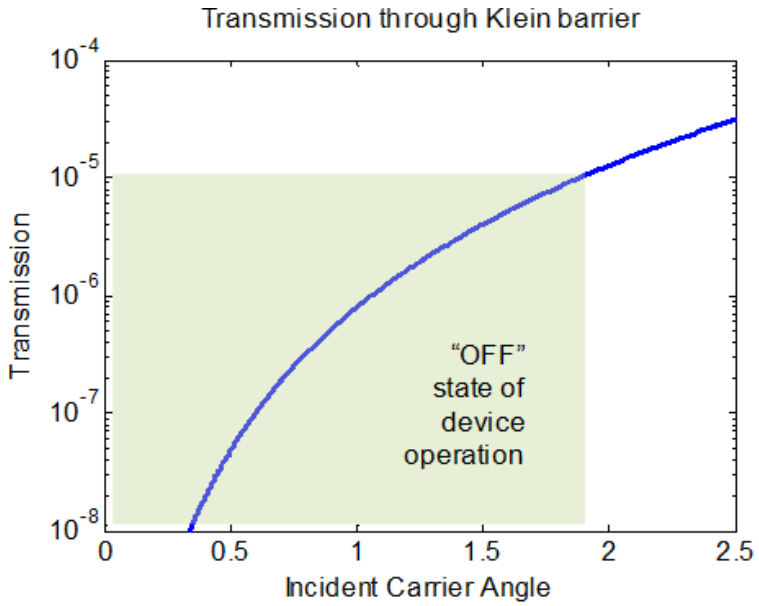

Figure 6.4: Transmission of carriers through a 41 nm wide energy barrier in BLG (for E / V = 108 meV / 209 meV). The transmission probability is plotted vs. incident carrier angle, θ. For θ_{max} = 1.89º, a single carrier out of 10^5 passes through the Klein barrier. That is, for θ <1.89º, I_{on}/I_{off} is > 10^5. This condition represents the *off* state of the device.

Next, the challenge of carrier collimation is discussed. The Klein effect predicts that carriers in BLG that strike an energy barrier at normal incidence are fully reflected. At small deviations from normal incidence, tunneling increases to a point such that the device no longer supports current modulation (leakage current becomes too high). Thus the capacity to direct a collimated beam of carriers to strike the Klein barrier at normal incidence is essential for device operation. It is assumed that contacts inject carriers into graphene at an angle that deviates up to 45° from the normal (the direction of carrier propagation is uniformly distributed within this cone of injected carriers). Then, requiring θ_{max} = 1.89º (to realize a current modulation of > 10^5), 1 out of 24 carriers injected into graphene is expected to contribute to transport. The aperture is realized by etching of a graphene slit at the junction of the metal and graphene. After passing through the slit, the collimated beam is preserved by a Kronig-Penney type potential—a periodic arrangement

of rectangular potential barriers—in the graphene lattice, termed a graphene super-lattice [116]. In total, three back-to-back p-n junctions are utilized. With a pitch of 10 nm between junctions, the super-lattice structure is 30 nm in length. The cost of the aperture and super-lattice on circuit speed and area is considered. The aperture increases both R_{on} and R_{off} by a factor of 24. Reflectance (R) of carriers through the super-lattice relates to θ through $R = \tan^2(\theta/2)$ [116]. Nonetheless, the structure increases overall channel length. In terms of area, the super-lattice structure introduces a 30% overhead to the graphene gate in comparison to the equivalent silicon gate. For graphene, a minimum size graphene inverter and NAND2 gate require an area of 8×17 and 13×17 F^2, respectively, where F is a given technology node's minimum size feature.

System-level performance of arithmetic logic units (ALUs) enabled by graphene Klein tunneling devices is benchmarked against the silicon CMOS platform. Specifically, latency, energy, and area are evaluated at the 32 nm technology node for (i) a 64-bit Brent-Kung (B-K) adder [117] and (ii) a 64-bit Kogge-Stone (K-S) adder [118]. The B-K and K-S adders are parallel-prefix carry look-ahead adders, composed of three stages: (i) pre-processing of generate ($g_i = a_i \cdot b_i$) and propagate ($p_i = a_i$ XOR b_i) bits, (ii) group carry generate ($G = G_{left} + G_{right} \cdot P_{left}$) and group carry propagate ($P = P_{left} \cdot P_{right}$), and (iii) post-processing: carry ($c_{i+1} = G + c_0 \cdot P$) and sum ($s_i = p_i$ XOR c_i). The B-K adder optimizes energy by reducing the number of group carry nodes while the K-S adder optimizes latency by achieving a minimal logic depth, Table 2. Both graphene and silicon ALUs use copper interconnects, whose properties are chosen from ITRS2009. Custom floor-plans are generated to estimate interconnect delay along the critical path and interconnect power dissipation throughout the circuit. These adders trade (with each other) latency for

energy, providing a strong basis to benchmark the performance of the Klein tunneling device. In the model, graphene adder differs from the silicon adder at the material and device levels while they are equivalent at the circuit and interconnect levels.

Table 2: Circuit comparison of B-K and K-S adders

Circuit Parameters	*Brent-Kung*	*Kogge-Stone*
Logic depth, n-bit	$2\cdot\log_2(n)-2$	$\log_2(n)$
Area, n-bit (group carry nodes)	$2\cdot n-2-\log_2(n)$	$n\cdot\log_2(n)-n+1$
Logic depth, 64-bit	10	6
Area, 64-bit (group carry nodes)	120	321

Circuit latency is computed by the method of stage effort (delay is normalized to the delay of an inverter driving an identical inverter, $\tau = 3{\cdot}RC$). Circuit power is the sum of dynamic, stand-by, leakage (tunneling via gate dielectric), and interconnect power.

$$\begin{aligned} P_{dynamic} &= \alpha \cdot f_{clk} \cdot \left(C_{logic} + C_{interconnect}\right) \cdot V_{DD}^2 \\ P_{standby} &= I_{standby} \cdot V_{DD}^2 \cdot C_{logic\_eff} \\ P_{leakage} &= I_{leakage} \cdot V_{DD}^2 \cdot C_{logic} \\ P_{total} &= P_{dynamic} + P_{standby} + P_{leakage} \end{aligned} \tag{6.5}$$

where α is activity factor, f_{clk} is clock frequency, C_{logic} is total logic capacitance, $C_{interconnect}$ is total interconnect capacitance, and C_{logic_eff} is effective logic capacitance based on the probability a device is in the *off* state (i.e. for $V_{ds} = V_{dd}$ and $V_{gs} = 0$). $I_{standby}$ is current in the *off* state and $I_{leakage}$ is a function of the gate dielectric and V_{gs}. Using Equation (6.5), energy per clock cycle is the product of power and clock period, i.e. the energy dissipated by the adder assuming it is a single-cycle adder (latency $< 1/f_{clk}$).

System-level metrics for the 64-bit B-K and K-S adders using both graphene and silicon implementations are compared in Table 3. The graphene K-S adder has a 38% and 77% reduction in latency and energy, respectively, over its silicon counterpart; the graphene B-K adder has a 52% and 81% improvement in latency and energy, respectively. While latency decreases for both types of adders, the improvement is more apparent for the B-K adder since a greater proportion of its delay hinges upon logic. The material, device, circuit, and interconnect parameters used in the model are shown in Table 4.

Table 3: Performance comparison of 64-bit B-K and K-S adders for graphene and silicon implementations at the 32 nm technology node

System Metrics	Latency (ps)	Gain (%)	Energy (pJ)	Gain (%)	Area (μm^2)
Ref [119]: Silicon K-S	180–190		6–8		
This model: Silicon K-S	220	--	4.53	--	119.9×23.7
This model: Graphene K-S	136	38 %	0.79	77 %	143.9×28.4
This model: Silicon B-K	324	--	4.22	--	108.7×25.1
This model; Graphene B-K	157	52 %	0.64	81 %	130.4×25.1

Table 4: Material, device, circuit, and interconnect properties used in model for graphene and silicon adders

Parameter	Silicon*	Graphene	
V_{dd} (V)	0.9	0.5	Material and Device Properties
Minimum width (nm)	41	41	
I_{on} (mA/μm)	1.5	2.16	
I_{off} (nA/μm)	500	22	
Gate EOT (nm)	1	2	
$I_{leakage}$ (A/cm^2)	0.1 [120]	0.01 [121]	
μ (cm^2/V-s)	--	2×104	
$\mu_{electron}/\mu_{hole}$	1	1	
0.69·RC (ps)	2.31	0.74	
α	0.2 [119]		Circuit
f_{clk} (GHz)	1		
pitch	41		Interconnect (Local)
Cu aspect ratio	1.8		
ρ (μΩ-cm)	4.08		
RC (ps/μm)	2.56		
pitch	90		Interconnect (Semiglobal)
Cu aspect ratio	1.5		
ρ (μΩ-cm)	3		
RC (ps/μm)	0.42		

* Material and device properties for silicon and circuit and interconnect properties common to silicon and graphene are obtained from ITRS2009

The rise of mobile platforms and cloud computing has refocused microproessor design around the tradeoff between performance and energy efficiency. Under this design paradigm, graphene delivers system-level benefits by enabling the speed-up of logic-

intensive, data processing units (or significant power savings at the same level of performance). The performance-power design space (in terms of power and latency) for the graphene B-K and K-S adders is shown in Figure 6.5. Herein, the requirement that $I_{on}/I_{off} > 10^5$ (preserved by fixing the aperture size such that $\theta < \theta_{max} = 1.89°$) is relaxed; instead, the aperture size is varied. Given a larger acceptance angle, both R_{on} and R_{off} reduce (now a greater proportion of carriers injected from the metal contacts can pass through the aperture) at the expense of increased leakage power. In other words, energy dissipation is traded for speed. The performance-power design space illustrates the effect of a device-level property (θ) on system-level performance. If θ is too large, tunneling through the Klein barrier becomes too high device operation.

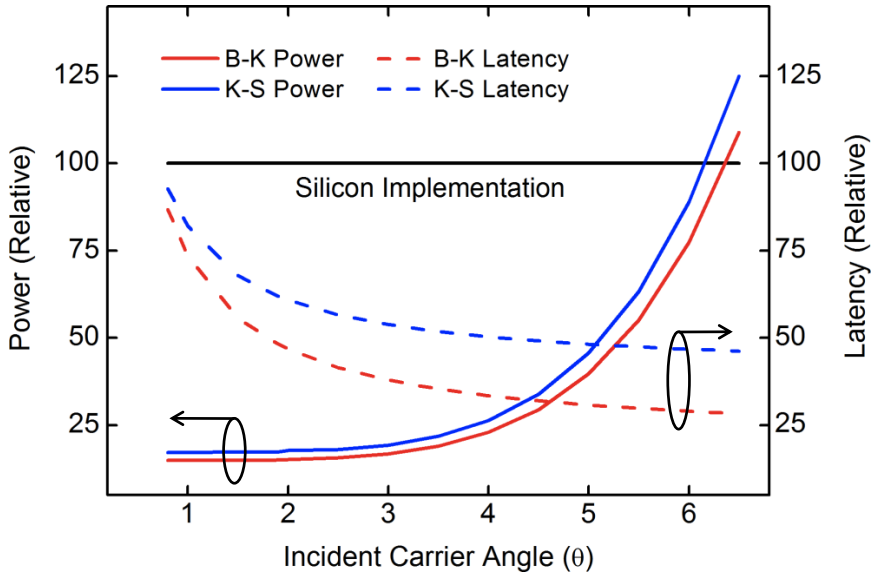

Figure 6.5: Performance-power design space for graphene B-K and K-S adders. This reveals that a device parameter—incident carrier angle θ—percolates up to the system-level performance of the ALUs. Power and latency for graphene adders are plotted with the silicon values (metrics for the graphene B-K adder are normalized to those of the silicon B-K adder while metrics of the graphene K-S adder are normalized to those of the silicon K-S adder). For $\theta > 6°$, the benefit of huge power savings disappears due to substantial leakage current.

6.4 Experimental Progress

The graphene Klein tunneling device needs to overcome several experimental challenges before it can be used in a practical device. These challenges fall under two general but related themes: (i) realization of high-mobility graphene and (ii) manufacture of high-resolution p-n junctions. First, an assumed mobility of 2×10^4 cm^2/V-s used to benchmark the Klein tunneling device in Section 6.3 is optimistic. While a mobility up to 2×10^5 cm^2/V-s at room-temperature is possible by suspending the graphene sheet [9], various external scattering sources appear in practical devices. The selection of SiO_2 as the dielectric imposes a mobility limit of 4×10^4 cm^2/V-s due to scattering from remote phonons [17]. Impurity and edge scattering further limit device performance. Second, the device demands the manufacture of p-n junction structures to be used as collimators and Klein barriers. These junctions need to be patterned with both high spatial and doping resolution. Notably, the edges of the junctions should be sharp compared to the Fermi wavelength (λ_F), expressed as $2\pi/k_F$ or $2\sqrt{(\pi/n)}$. A check reveals that λ_F remains above 10 nm for doping levels as high as ~10^{13} cm^{-2}, larger than LER (2–3 nm) from lithographic patterning.

Previous experimental studies on Klein tunneling in graphene involved diffusive [122] and ballistic [123] transport through graphene n-p-n structures. In the diffusive study, the measured transmission represents an average transmission across different angles. In the ballistic study, Fabry-Perot resonances are observed as a result of interference of multiple reflections at the junction interfaces. While these studies have provided evidence for the Klein effect in graphene, there has yet to be a direct study on key experimental issues of a Klein tunneling device. This section explores the feasibility

of graphene p-n junction structures manufactured by chemical doping (chemical doping permits more aggressive scaling than electrostatic doping). In previous work from the group [124], a method to dope 2D, large-area graphene via e-beam lithography using HSQ was developed. As a result of a change in the structure of HSQ by adding external energy [57] (upon e-beam exposure in this case), the resist hole- or electron-dopes graphene depending on e-beam dose. This doping method is optimized for 1D graphene ribbons, thus enabling the manufacture of high-resolution p-n junctions. The efficacy of this doping method is confirmed by electrical testing for 200 nm wide GNRs, Figure 6.6. The range of Dirac points, from –20 to +30 V, correspond to a range of doping densities from -1.4×10^{12} cm^{-2} (n-doping) to $+2.1\times10^{12}$ cm^{-2} (p-doping). Herein, different ribbons are assigned different EBL doses but for each ribbon, uniform doping is applied. After EBL exposure, the HSQ film is developed in 2.38% TMAH for 70 sec. The devices are then exposed to an argon plasma etch to transfer the HSQ pattern into the graphene sheet. A transition from n-type to p-type doping occurs under the range of applicable doses, allowing complementary doping of 1D graphene. Using these results, the device engineer can selectively dope regions of graphene to be p- or n-type in a single lithography step. The method of local chemical doping of graphene via HSQ has been extended to ribbons as narrow as 100 nm.

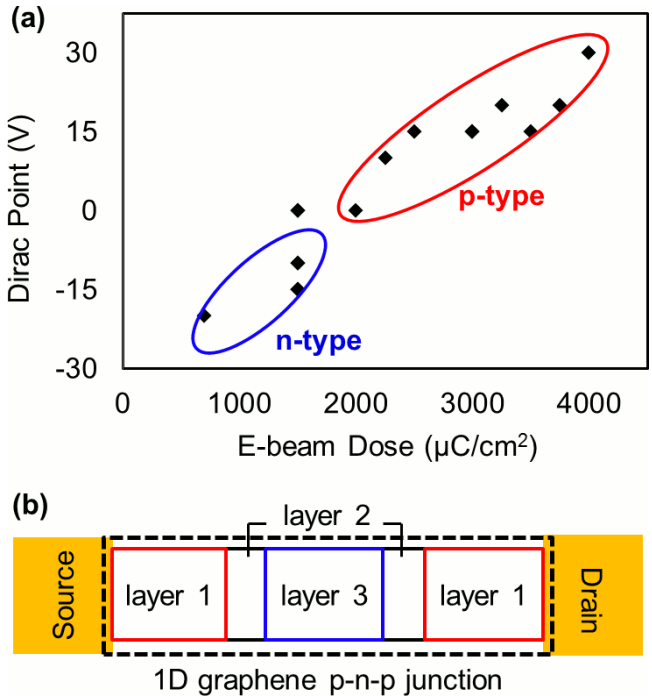

Figure 6.6: Localized chemical doping of graphene via HSQ. In (a), the Dirac point for 200 nm wide GNRs vs. EBL dose (using HSQ resist) is shown. The Dirac point for a device is the gate voltage at the minimum conductivity point. Different ribbons are assigned different EBL doses but for each ribbon, uniform doping is applied. Devices are then exposed to an argon plasma for 5 sec. to etch the HSQ patterns into graphene. In (b), this doping method is integrated into the fabrication process of p-n-p junctions by selective EBL exposure in different sections of the graphene ribbon.

This chemical doping method is used to manufacture high-resolution graphene p-n junctions. To look for evidence of angle-dependent transport in Klein devices, energy barriers are patterned at different angles with respect to the length of the device. Figure 6.7 shows the I-V data for five p-n-p junction devices (two with collimators and three with Klein barriers). The presence of two resistance maxima across the devices reveals the formation of graphene p-n junctions. However, the differences between the transport of R1–R2 (designed with collimators) and R3–R5 (designed with Klein barriers) are not detected. Herein, device dimensions are still larger than the carrier mean free path, which is around 100 nm for high-quality graphene devices. Scaling of p-n junctions to the sub-

100 nm length scale is thus needed to operate the device in the ballistic regime and see evidence of Klein tunneling.

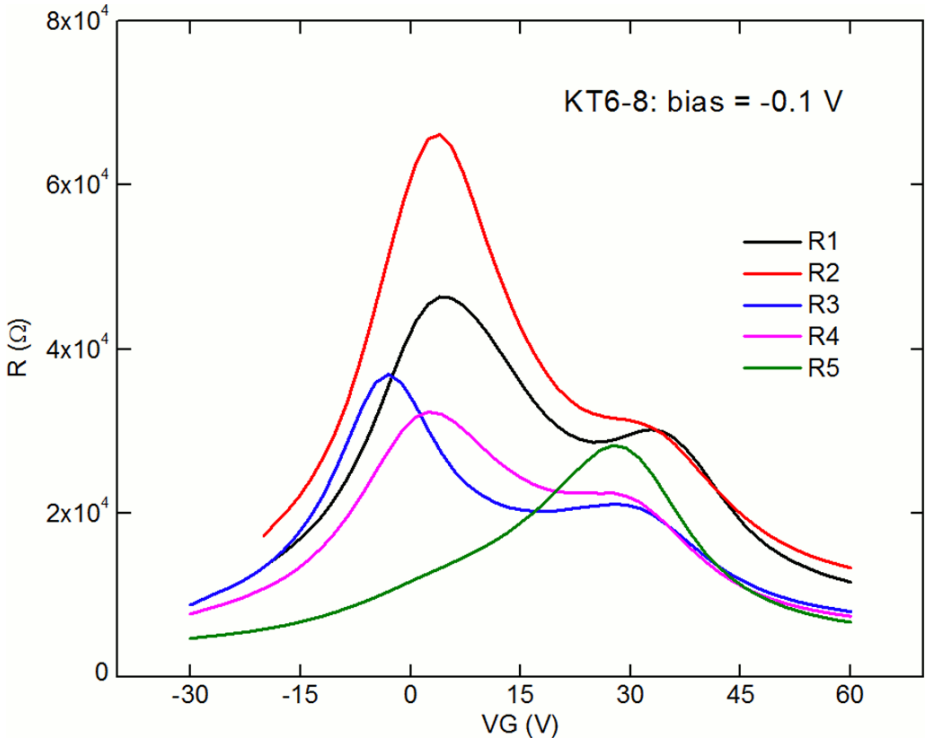

Figure 6.7: I-V behavior of p-n-p junction devices on single-layer graphene. Two of the devices (R1–R2) have a junction patterned perpendicular to the direction of transport (thus acting as collimators). The other three devices (R3–R5) have a junction patterned diagonal to the direction of transport (thus acting as Klein barriers). Each device has a width of 200 nm and length of 500 nm. The display of two resistance peaks reveals the formation of graphene p-n junctions.

6.5 Conclusions

The Dirac physics of graphene directs carriers to behave in a light-like manner. As a result, carriers that traverse graphene p-n junctions undergo reflection, refraction, or transmission in analagous fashion to the way photons traverse different materials. This property can be exploited to build a novel device concept in graphene without the need for a bandgap. In this work, device-level prospects of a graphene Klein tunneling device are analyzed. The device uses a gate to control transport across graphene p-n junctions,

much like the case for a silicon field-effect device, except that the gate in the graphene device actuates a relativistic tunneling effect. At the system level, graphene/Klein-based chips are benchmarked against conventional silicon/CMOS-based chips. B-K and K-S adders are analyzed and a significant improvement is found for the graphene chips in terms of latency and energy dissipation. The engineering tradeoffs at the device level for which performance of the graphene adder exceeds that of the silicon adder are illustrated. Lastly, the feasibility of the Klein tunneling device is explored through use of chemical doping method to manufacture graphene p-n junctions. The efficacy of HSQ doping of graphene is demonstrated for graphene ribbons as narrow as 100 nm. Improvements in the synthesis or patterning of graphene are needed for the device to become practical.

CHAPTER 7

SUMMARY AND RECOMMENDATIONS

7.1 Research Summary

This thesis explores the potential for graphene as a material and technological platform for electronics, and is divided into two themes. In the first theme, fundamental physical and structural properties of graphene as it evolves from 2D (large-area) form to 1D (GNR) form are investigated. Such graphene structures are of interest to the device community because of the possibility of bandgap engineering and, thus, graphene-based FETs. In the second theme, a beyond-FET device concept is advanced to better suit the unique physics of graphene. This device concept is based on the Klein paradox, which predicts angle-dependent tunneling through graphene p-n junctions.

Task 1: Technology Development of Graphene Devices

Methods for the design, fabrication, and characterization of graphene devices are developed and qualified. This work flow was first established for graphene devices built on the field-effect concept. It is used later as a baseline to develop an alternative work flow: graphene p-n junctions devices based on the Klein tunneling effect. In the former device concept, EBL is used to pattern ultra-narrow GNRs. In the latter concept, EBL is used to pattern graphene p-n junctions through chemical doping.

Task 2: Current-Carrying Capacity and Thermal Management in Graphene Devices

Graphene devices are shown to exhibit an impressive breakdown current density and thermal conductivity. EBL is used to pattern devices consisting of a set of GNRs of

widths between 16 and 52 nm and lengths between 0.2 and 0.75 μm. Of 21 devices tested in this study, a majority of GNRs exhibit $J_{BR} > 1$ μA/nm^2 while a handful exhibit $J_{BR} > 10$ μA/nm^2. Breakdown current density is found to have a reciprocal relation with device resistivity. In addition, these devices show good thermal properties: high-quality GNRs exhibit a k upward of 800 W/m-K. These findings have important benefits for graphene as an electronic material. First, a high current-carrying capacity allows device operation at increased voltages and currents. Second, a high thermal conductivity aids the thermal management of graphene devices.

Task 3: Size Effect in Nanoscale Graphene Devices

Carrier confinement in GNRs leads to a width-dependent bandgap, providing a route toward graphene FETs. In realistic GNRs, rough edges lead to edge scattering. The more aggressively that GNRs are scaled, the larger the impact of their edges, whose LER is roughly 2–3 nm from lithographic patterning. The electrical impact of the size effect is measured by correlating GNR mobility to width. In this study, while a mobility of 2000-4000 cm^2/V-s is realized for W > 50 nm (limited by impurity scattering), this decreases to less than 200 cm^2/V-s for $W < 20$ nm (limited by edge scattering). The crossover between impurity-limited mobility and LER-limited mobility occurs at a width of ~50 nm. In other studies, this onset of the size effect is seen at different widths because of differences in edge roughness and impurity density of the GNRs. In addition, a process flow, based on the selective hydrogenation of carbon atoms at the edges of a GNR device, is developed as a way to mitigate the electrical impact of the size effect. Electrical testing of edge-passivated GNR devices show an improvement in carrier mobility.

Task 4: Variation in Graphene Devices

Owing to its atomically thin nature, graphene is an extremely sensitive material. To investigate device variability, two sources of variation are studied: (i) atmospheric adsorbates in exfoliated graphene on SiO_2 and (ii) substrate-induced disorder in epitaxial graphene on SiC.

Exfoliated graphene, after exposure to oxygen or ambient air, becomes strongly hole-doped. In this study, mobility varies from 1000–4000 cm^2/V-s and can be improved or degraded depending on the nature of the substrate impurities. A model is derived to understand the interplay between the adsorbate layer and the substrate impurity layer. It is posited that atmospheric adsorbates mitigate scattering from negatively charged substrate impurities but cause increased scattering from positively charged substrate impurities. That doping rates under O_2 (ambient) exposure are inversely proportional to (independent of) graphene thickness suggests that O_2 (ambient) doping occurs on the basal plane (at the edges) of the graphene sheet.

In epitaxial graphene (grown on the Si-face), substrate disorder leads to ridge-like terrace steps across the graphene film. In addition, the film thickness is non-uniform: typically, SLG grows within terraces while BLG grows at the terrace steps. This property, combined with the fact that SiC substrate and interface layer (between graphene and the substrate) strongly electron-dope graphene, produces a multi-modal carrier distribution across the film. An anisotropic transport behavior is thus observed.

Task 5: Identification and Analysis of a New Device Platform: Graphene p-n Junctions

The mutual dependence of a graphene device and its manufacturability demands the integration of material, device, and architectural solutions. It is thus vital to consider the unique features of graphene to develop a suitable platform. Herein, a device concept

built around the Dirac physics of graphene is discussed. In particular, the governing of transport in graphene by Dirac physics leads to an angle-dependent tunneling effect, the so-called Klein tunneling effect. Device- and system-level benefits of a bi-layer graphene Klein device are demonstrated. The feasibility of this device is experimentally assessed by exploring chemical doping; chemical method, compared with electrostatic doping, facilitates a smaller footprint in the manufacture of Klein devices. Herein, the efficacy of HSQ doping of nanoscale graphene is demonstrated.

7.2 Future Work

At the start of this research effort (back in 2008), the study of graphene and its logic applications were just getting started. It has thus been a tremendous opportunity to do research in such an open and creative environment. The findings of this thesis signal future opportunities for graphene as a semiconductor material, and are discussed from a short-term (immediate follow-up work) and long-term (in a broader sense) view.

The mitigation of the size effect can be achieved via the synthesis or patterning of graphene ribbons with greater precision to reduce LER or passivation of rough edges to reduce the negative impact of these edge states on transport. Preliminary analysis on the passivation of GNR edges via hydrogenation shows up to a 50% increase in mobility of the ribbons. Herein, more work is needed to improve the efficacy of the hydrogenation process for GNR devices. More generally, this hydrogenation study is part of a broader effort in the research community to develop methods for the chemical functionalization of graphene. This chemical functionalization, both covalent and non-covalent, provides opportunities for chemical tailoring of electronic transport properties [125]. Covalent

functionalization (e.g., by fluorination or hydrogenation) can be used to convert targeted areas from semi-metallic to insulating graphene; non-covalent functionalization (e.g., by surface adsorption of salt solutions) can be used to dope graphene. Extending this idea, an all-graphene chip can be realized with graphene as the semiconducting material for logic, the conducting material for interconnects, and the insulating material for isolation and/or passivation of conductive regions.

Epitaxial graphene grown on SiC(0001) reveals thickness and doping variation, which leads to the formation of p-n junctions. This raises an interesting prospect—is it possible to leverage these naturally occurring p-n junctions as a bottom-up fabrication method for graphene p-n junctions? Such a prospect depends on the proper engineering of the growth conditions of epitaxial graphene in order to control the properties of the terrace structures. For instance, the dimensions of the terrace step edges determines the dimensions of the BLG regions near those steps (in the work of this thesis, the BLG regions have a width, or spatial resolution, on the order of 100 nm). Much work is needed to characterize the effect of various growth conditions (e.g., in vacuum or in a pressurized environment, at what temperature, etc.) on the size of the terraces and its step edges. Such a bottom-up fabrication method for graphene p-n junctions is attractive since the critical dimensions of the junctions would not be determined by lithographic patterning but rather by natural growth mechanisms.

In the Klein effect study, the next step requires the scaling of p-n junctions to the sub-100 nm length scale to operate the device more wholly in the ballistic regime. This involves (i) further reduction of scattering sources in the graphene devices (e.g., using hexagonal BN instead of SiO_2 as the substrate to reduce remote phonon scattering) and

(ii) characterization of the HSQ doping method for sub-100 nm GNRs. Going forward, it appears that digital logic applications in graphene would be better suited for a beyond-FET device concept. However, it should be noted that graphene FETs still remain an attractive platform for analog/RF applications [126]. RF devices operate in the direct-current *on* state with small RF signals superimposed onto the direct-current signals. As a result, a graphene RF device can exploit the material's superb mobility and robustness to short-channel effects without being severely constrained by energy consumption.

7.3 Outlook

As research and development of the synthesis and properties of graphene grow and diversify, the potential applications are tantalizing. While much of this potential from an electronics perspective remains untapped, it is noted that graphene was first isolated less than 10 years ago. Graphene is a remarkable material but a significant, coordinated engineering effort is needed to deliver practical graphene products. In the semiconductor industry, graphene is competing with decades of development of silicon technology as well as its associated industrial ecosystem. Simply put, the competitive advantage of silicon against any new semiconducting material is tremendous. The success of graphene electronics thus depends to a large extent on the success of graphene in other industries (to build economies of scale for the graphene industry). The earliest graphene products to hit the market are likely to be those in which graphene quality (in terms of purity) is not essential. In semiconductors, miniaturization and very-large-scale-integration of devices require very precise control of material and device quality. But for mechanical or thermal systems at the macroscopic scale, material quality can be sacrificed for manufacturing

cost and throughput. As an example, graphene will likely be used soon in composite materials to strengthen and/or reduce the weight of the material. Applications include sporting goods (clubs or rackets) and military equipment (body armor or helmets). Once such products make it into the market, they will inevitably drive down manufacturing costs for other graphene applications and improve the overall industrial ecosystem that supports graphene.

Appendix A: Process Flow for Exfoliated Graphene Devices

Start wafer: 300 nm thermally-grown SiO_2 on p++ Si (4" diameter); resistivity in range of 0.001–0.005 mΩ-cm. Backside oxide film is etched to allow for back-gating. Vendor: University Wafers (batch of 25).

PREPARATION FOR GRAPHENE SYNTHESIS
Objective: batch process a 4" wafer into "piece" wafers (dimensions ~1 cm^2; suitable for working with exfoliated graphene) with alignment markers to help identify and pattern graphene flakes after exfoliation.

1. **Optical mask: for subsequent photolithography**
   - Design. A single "piece" wafer consists of a 20×20 grid of alignment markers with 500 μm pitch in both x and y. This gives a total grid area of 9.5×9.5 mm^2. The dimensions of a piece wafer are chosen to be amenable to the exfoliation process (e.g., the width of tape used) and to the e-beam lithography step (e.g., the width of the cassette window used for the EBL exposure). Meanwhile, each alignment marker features two rectangles (10×50 μm^2) that overlap perpendicular to one another to form a cross-hair pattern. The spacing between the edge of one piece wafer to the closest edge of its adjacent piece wafer is 2 mm, giving a pitch of 11.5 mm from one piece wafer to the next. This spacing is included for ease of dicing the 4" wafer and subsequent handling of the piece wafers.
   - Fabrication: 5" dark-field quartz mask is purchased from Photo Sciences, Inc.

2. **Photolithography: pattern alignment markers into resist**
   - Start wafer: 300 nm thermally-grown SiO_2 on p++ Si (4" diameter)
   - Wafer clean: AMI—spray acetone, methanol, and IPA for 1 min. each; N_2 dry
   - Mask clean: AMI—spray acetone, methanol, and IPA for 1 min. each; N_2 dry
   - Spin-coat: 1827 resist at 3000 RPM for 30 sec. (500 RPM/sec ramp)
   - Pre-bake: 115 °C for 8 min. in oven
   - Equipment: Karl Suss TSA MA6 Mask Aligner (Marcus inorganic cleanroom)
   - Exposure settings:
     - Channel selection: 2 (405 nm UV lamp)
     - Dose (a function of resist type and thickness): 450 mJ/cm^2; thus exposure time is lamp power (in units of mW/cm^2) divided by dose
     - Contact type: vacuum
     - Alignment gap: 25 μm
   - Post-bake: 115 °C for 1 min. in oven
   - Develop: MF-319 bath for 1 min. with gentle agitation; rinse under DI tap for several seconds then place wafer in DI bath for 1 min.; N_2 dry
   - Inspection: optical microscopy to check integrity of features. If features are underdeveloped, place wafer back into MF-319 bath for 30 sec., rinse, and re-inspect. Continue this process until features are fully developed. If, after 4–5 min. of cumulative develop time, features remain underdeveloped then the wafer was significantly underexposed. In this scenario, strip the resist using 1165 and re-start the photolithography step.

- Mask clean: AMI—spray acetone, methanol, and IPA for 1 min. each; N_2 dry

3. **E-beam evaporation and resist/metal liftoff: fabricate metal alignment markers using resist pattern**
   - Descum: etch residual resist before evaporation to promote better adhesion between metal and oxide substrate
   - Metal source clean: AMI—use texwipe to wipe down both metal source and its crucible using acetone, methanol, and IPA
   - Sample holder (plate) clean: AMI—use texwipe to wipe down sample holder using acetone, methanol, and IPA
   - Equipment: CVC 1 E-beam Evaporator (Pettit cleanroom)
   - Evaporation settings:
     - Shutter control: manual mode
     - Pressure: pump down chamber to ~10^{-6} Torr. Ti gettering lowers pressure to 7–8×10^{-7} Torr before deposition begins; heating of Au increases it to 2–3×10^{-7} Torr before deposition begins.
     - Deposition: 10/70nm Ti/Au thickness with 0.5/1.0 Å/s deposition rate. Use manual shutter control to keep the shutter between the metal source and evaporation target (wafer) for one min. after tool goes into deposition mode. This mitigates any effects of contamination on the surface of the metal source (since these contaminants are burned off before actual deposition begins).
     - Vent: wait 8 min. before starting N_2 vent to prevent oxidation of source metals
   - Liftoff: 1165 bath at 140 °C for ≥ 1 hr.
   - Wafer clean: AMI—spray with acetone for 1 min. then soak in methanol and IPA for 1 min. each; N_2 dry. Importantly, during acetone spray, hold wafer at slant or upside down so the stripped metal and other particulates do not fall back to substrate. If portions of the resist/metal stack do readily lift off then apply a vigorous acetone spray.

4. **Dicing: cut 4" wafer into piece wafers**
   - Protect top-side of wafer: spin-coat 1827 resist (same settings as for photolithography step)
   - Equipment: Pettit Dicing Saw
   - Dicing settings:
     - Blade: choose smallest blade (made of Ni) with 50 μm blade tip radius
     - Pitch: 11.5 mm in both x and y
   - Liftoff: 1165 bath at 140 °C for ≥ 15 min.
   - Wafer clean: AMI—spray with acetone for 1 min. then soak in methanol and IPA for 1 min. each; N_2 dry

STANDARD GRAPHENE DEVICE PROCESS FLOW

1. **Exfoliation: production of graphene flakes from bulk graphite**
   - Start wafer: 300 nm thermally-grown SiO_2 on p++ Si (piece wafer)

- Wafer clean: AMI—spray acetone, methanol, and IPA for 1 min. each; N_2 dry. Then run descum process to remove organic residue on wafer surface. Finally, dehydrate wafer in Heraeus vacuum oven at 300 °C for 1 hr.
- Graphite source: Kish A purchased from Toshiba Ceramics.
- Tape: moderate-tack tape (e.g., 3M Scotch tape)
- Flaking process: place (thick) graphite flakes onto fresh piece of tape. Fold tape over itself to thin down graphite (in which there is a higher probability of finding single-, bi-, or few-layer graphene). Alternatively, use a fresh piece of tape to thin down graphite on original piece of tape. Once the graphite is sufficiently thinned down, place tape on top of wafer. Timing here is critical as this tape should be applied to the wafer immediately after wafer is removed from oven or hot plate. Ensure tape is flush with surface of wafer by rubbing the tape/wafer with a cotton swab. Avoid air bubbles. Finally, gently peel away tape from wafer—go at a very slow pace (it should take up to 1 min. to completely remove the tape).
- Flake identification: use microscope to find location of flakes relative to pre-patterned alignment markers on the substrate. These coordinates will be used later during e-beam lithography patterning.
- Metrology—Raman: verify thickness and quality of graphene flakes
  - Equipment: Thermal Scientific Raman Spectrometer
  - Laser selection: 488 nm

2. E-beam lithography layer 1: pattern contact electrodes into resist

- Design: contact electrodes to a single flake consist of at least four electrodes to yield at least one device with a four-point configuration per flake. Typically flake size is on the order of 10×5 μm^2, and EBL alignment tolerance (using alignment markers defined by photolithography) is on the order of 0.5 μm. In addition to contact electrodes, additional alignment markers are patterned to improve alignment tolerance for subsequent EBL patterning.
- Spin-coat: ZEP520A resist at 2000 RPM for 60 sec. (500 RPM/sec ramp)
- Pre-bake: 180 °C for 2 min. on hot plate
- Equipment: JEOL JBX-9300FS E-beam Lithography System (Pettit cleanroom)
- Exposure settings:
  - Current: 2 nA
  - Calibration: normal1
  - Shot pitch: 4 nm
  - Base dose: 400 $\mu C/cm^2$
- Post-bake: none
- Develop: amyl acetate bath for 2 min. with gentle agitation; rinse by IPA spray for several sec. then place in IPA bath for 2 min.; N_2 dry
- Inspection: optical microscopy to check integrity of resist features

3. E-beam evaporation and metal liftoff: deposit contact electrodes

- Descum: etch residual resist before evaporation to promote better adhesion between metal and oxide substrate
- Metal source clean: AMI—with texwipe, wipe down both metal source and its crucible using acetone, methanol, and IPA

- Sample holder (plate) clean: AMI— with texwipe, wipe down sample holder using acetone, methanol, and IPA
- Equipment: CVC 1 E-beam Evaporator (Pettit cleanroom)
- Evaporation settings:
  - Shutter control: manual mode
  - Pressure: pump down chamber to ~10^{-6} Torr. Ti gettering lowers pressure to 7–8×10^{-7} Torr before deposition begins; heating of Au increases it to 2–3×10^{-7} Torr before deposition begins.
  - Deposition: 10/70nm Ti/Au thickness with 0.5/1.0 Å/s deposition rate. Use manual shutter control to keep the shutter between the metal source and evaporation target (wafer) for one min. after tool goes into deposition mode. This mitigates any effects of contamination on the surface of the metal source (since these contaminants are burned off before actual deposition begins).
  - Vent: wait 8 min. before N_2 vent to prevent oxidation of source metals
- Liftoff: 1165 bath at 140 °C for ≥ 1 hr.
- Wafer clean: AMI—spray with acetone for 1 min. then soak in methanol and IPA for 1 min. each; N_2 dry. Importantly, during acetone spray, hold wafer at slant or upside down so the stripped metal and other particulates do not fall back onto substrate. If portions of the resist/metal stack do not readily lift off then apply a vigorous acetone spray. However, *do not* in any circumstances use the ultrasonic bath with any solvent cleans of the wafer as this will knock graphene flakes loose from the substrate.
- Inspection: optical microscopy to check integrity of contact electrodes. Also need to identify the EBL-defined alignment markers to be used for subsequent patterning.
- Metrology—electrical test: verify EBL layer 1 alignment and quality of 2D, large-area graphene flakes
- Metrology—SEM imaging (*conditional*): verify adhesion and purity of contact electrodes. *This step is performed in the condition that, upon optical inspection, devices are contaminated with metal impurities or, upon electrical test, devices are highly resistive.*

4. E-beam lithography layer 2: pattern graphene structures into resist

- Design: graphene structures include both 2D, large-area graphene and 1D GNRs. Ribbons typically are constructed with a set of ten parallel ribbons to minimize ribbon-to-ribbon variation. In this scenario, each set of these ten parallel lines is considered a single device. EBL alignment tolerance (using alignment markers defined by EBL) is less than 0.1 μm.
- Spin-coat: 2% HSQ resist (XR-1541-002) at 5000 RPM for 60 sec. (2000 RPM/sec ramp)
- Pre-bake: 180 °C for 3 min. on hot plate
- Equipment: JEOL JBX-9300FS E-beam Lithography System (Pettit cleanroom)
- Exposure settings:
  - Current: 2 nA
  - Calibration: normal1

- Shot pitch: 2 nm (minimum shot pitch for 2 nA current, 50 MHz blanking amplifier, and 1000 $\mu C/cm^2$ base dose is 2 nm)
- Base dose: 1025 $\mu C/cm^2$ (slightly higher to account for drift in current)

- Post-bake: none
- Develop: MF-319 bath for 70 sec; 9:1 DI:MF-319 bath for 1 min; DI bath 1 for min; N_2 dry
- Inspection: optical microscopy to check integrity of resist features
- Metrology—electrical test
- Metrology: SEM imaging (*conditional*): verify EBL layer 2 alignment. *This step is performed under the conditional that, upon optical inspection, devices appear to be contaminated or, upon electrical test, devices are highly resistive.*

5. Etching: etch graphene flakes using resist pattern

- Design: minimize etch time to avoid unintentional doping of graphene via plasma
- Equipment: STS SOE.
- Pre-clean: run O2-CLEAN.set on silicon carrier wafer for 30 min.
- Calibration: run IY-ARG.set on calibration wafer (coated with ZEP resist) to monitor etch rate**.** Find ZEP thickness using Nanospec Refractometer.
- Process settings:
  - Recipe: IY-ARG.set
  - Etch time: 5–10 sec (etch rate is ~1 nm/sec)
  - Power: Platen 1 = 50 W; Platen 2 = 200 W
  - Gas: Argon with 20 sccm flow rate
  - Pressure: 5×10^{-3} Torr
- Post-clean: O2-CLEAN.set on silicon carrier wafer
- Inspection: optical microscopy to verify that flakes have been etched
- Electrical test: verify alignment and integrity of graphene structures
- SEM imaging (*conditional*): verify adhesion and purity of contact electrodes. *This step is performed under the conditional that, upon optical inspection, devices appear to be contaminated or, upon electrical test, devices are highly resistive.*

Appendix B: Influence of Atmosphere on Electrical Transport in Graphene—Parameters of the Resistor Network Model

Graphene sheets are modeled as distinct p- and n-regions that arise from charge puddles on the substrate. The expression of conductivity in each region is adapted from [29] and reproduced here

$$\sigma_{ds}(V_{gs}) = \begin{cases} \sigma_{\min} & if \quad V_{BG} - V_{g,\min} \le V^* \\ \sigma_{\min} + s \cdot (\ |V_{BG} - V_{g,\min}| - V^*\ ) & if \quad V_{BG} - V_{g,\min} > V^* \end{cases} \tag{B.1}$$

The model parameters used to describe the doping behavior of graphene exposed to the atmosphere are shown below for the experiments in case-2 through case-4.

Table 5: Parameters used to model the doping behavior of graphene to the atmosphere

σ_{ds} (V_{gs})		*Start of Doping*			*End of Doping*		
		$V_{g,min}$ (V)	σ_{min} (e^2/h)	s	$V_{g,min}$ (V)	σ_{min} (e^2/h)	s
Case-2 (sample D1) is modeled as p-, n-, p-regions in series	*p-region*	10	6	0.33	40	3.8	0.42
	n-region	-38	3.8	0.35	8	10	0.28
Case-3 (sample D2) is modeled as p-, n-regions in series	*p-region*	8	3.2	0.24	31	2.2	0.26
	n-region	-27	15	0.70	-4	13	0.50
Case-4 (sample D3) is modeled as n-, p-, n-regions in series	*p-region*	14	20	0.16	45	28	0.30
	n-region	-16	6.5	1.8	15	6.5	0.85

Appendix C: Matlab Code to Calculate Tunneling Probability of Carries Through an n-p-n Junction in Bi-layer Graphene

```
%% Klein Tunneling in BLG %%

clear all

%% constants

hbar=1.05457e-34; h=2*pi*hbar; m=9.10938e-31;q=1.60218e-19; k=8.61732e-5;
eps0=8.854e-12; m_BLG=0.033*m;

%% system parameters

D=41e-9; % width of klein barrier (i.e., width of p-region in npn junction), in m
V1=q*-0.108;V2=q*0.101;V3=q*-0.108;E=q*0.0; % potential across npn junction
s1=sign(V1-E);s2=sign(V2-E);s3=sign(V3-E); % sign of potential across npn junction

theta=[];

for j=1:10000
        theta(j)=j/1000;
        phi1=j/1000;phi2=phi1;phi3=phi1; % carrier angle with respect to the barrier
        normal, in deg.
        k1x=sqrt((2*m*abs(E-V1)))*cos(phi1*pi/180)/hbar; % kx of left region
        k2x=sqrt((2*m*abs(E-V2)))*cos(phi2*pi/180)/hbar; % kx of middle region
        k3x=sqrt((2*m*abs(E-V3)))*cos(phi3*pi/180)/hbar; % kx of right region
        k1y=sqrt((2*m*abs(E-V1)))*sin(phi1*pi/180)/hbar; % ky of left region
        k2y=sqrt((2*m*abs(E-V2)))*sin(phi2*pi/180)/hbar; % ky of middle region
        k3y=sqrt((2*m*abs(E-V3)))*sin(phi3*pi/180)/hbar; % ky of right region
        kap1x=sqrt((k1x^2+2*k1y^2)); % kapx of left region
        kap2x=sqrt((k2x^2+2*k2y^2)); % kapx of middle region
        kap3x=sqrt((k3x^2+2*k3y^2)); % kapx of right region
        h1=(sqrt((1+(sin(phi1*pi/180))^2))-sin(phi1*pi/180))^2;
        h2=(sqrt((1+(sin(phi2*pi/180))^2))-sin(phi2*pi/180))^2;
        h3=(sqrt((1+(sin(phi3*pi/180))^2))-sin(phi3*pi/180))^2;
        A1=[1, 1, -1, -1, -1, -1, 0, 0];
        A2=[-1i*k1x, kap1x, -1i*k2x, 1i*k2x, -kap2x, kap2x, 0, 0];
        A3=[0, 0, exp(1i*k2x*D), exp(-1i*k2x*D), exp(kap2x*D), exp(-kap2x*D), -
        exp(1i*k3x*D), -exp(-kap3x*D)];
        A4=[0, 0, 1i*k2x*exp(1i*k2x*D), -1i*k2x*exp(-1i*k2x*D),
        kap2x*exp(kap2x*D), -kap2x*exp(-kap2x*D), -1i*k3x*exp(1i*k3x*D),
        kap3x*exp(-kap3x*D)];
```

```
        A5=[-exp(-2*1i*phi1*pi/180), h1, -exp(2*1i*phi2*pi/180), -exp(-
        2*1i*phi2*pi/180), h2, 1/h2, 0, 0];
        A6=[1i*k1x*exp(-2*1i*phi1*pi/180), kap1x*h1, -1i*k2x*exp(2*1i*phi2*pi/180),
        1i*k2x*exp(-2*1i*phi2*pi/180), kap2x*h2, -kap2x*1/h2, 0, 0];
        A7=[0, 0, exp(1i*k2x*D+2*1i*phi2*pi/180), exp(-1i*k2x*D-2*1i*phi2*pi/180),
        -h2*exp(kap2x*D), -1/h2*exp(-kap2x*D), exp(1i*k3x*D+2*1i*phi3*pi/180), -
        1/h3*exp(-kap3x*D)];
        A8=[0, 0, 1i*k2x*exp(1i*k2x*D+2*1i*phi2*pi/180), -1i*k2x*exp(-1i*k2x*D-
        2*1i*phi2*pi/180), -kap2x*h2*exp(kap2x*D), kap2x*1/h2*exp(-kap2x*D),
        1i*k3x*exp(1i*k3x*D+2*1i*phi3*pi/180), kap3x*1/h3*exp(-kap3x*D)];
        A=[A1;A2;A3;A4;A5;A6;A7;A8];
        B=[-1;-1i*k1x;0;0;exp(2*1i*phi1*pi/180);1i*k1x*exp(2*1i*phi1*pi/180);0;0];
        x=inv(A)*B;
        T(j)=(abs(x(7)))^2;
end

axes('FontSize',12);
semilogy(theta,T,'linewidth',2);
xlim([0 10]); ylim([1e-8 1e-2]);
```

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